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Design and Analysis of Asymmetric Sleepy Stack SRAM for Reduction of Leakage Power

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Abstract: Leakage power is a major issue for short channel devices. As the technology is shrinking (i.e., 180nm, 90nm, 45nm , 22nm etc) the leakage current is increasing very fast. So, several methods and techniques have been proposed for leakage power reduction in CMOS digital integrated circuits Leakage is a serious problem particularly for CMOS circuits in nanoscale technology. We propose a novel ultra-low leakage CMOS circuit structure which we call "Asymmetric Sleepy Stack." Unlike many other previous approaches, Asymmetric sleepy stack can retain logic state during sleep mode while achieving ultra-low leakage power consumption. We apply the Asymmetric sleepy stack to generic logic circuits. Although the sleepy stack incurs some delay and area overhead, the Asymmetric sleepy stack technique achieves the lowest leakage power consumption among known state-saving leakage reduction techniques, thus, providing circuit designers with new choices to handle the leakage power problem.

Key words— Sub-Micron, Critical path delay, Leakage power Dissipation, Supply Voltage and Threshold Voltage.

1. INTRODUCTION

According to Moore's law, the number of transistors integrated per square inch on a die has doubled every 18 months, since the integrated circuit was invented. Also, every few years the size of the transistors employed is shrunken and the frequency of circuits increases. As these trends continue, several new challenges become relevant in implementing of Very Large Scale Integrated (VLSI) circuits. With the advance of semiconductor manufacturing technology, the Requirements of VLSI circuits have led to many challenges during manufacturing process .

Memory is an important part of computer and microprocessor based system design. It is used to store data or information in terms of binary number (0 or 1). The data that is used for programs and the program code are also stored in the memory. Memory is required for temporary as well as permanent storage of data in digital system. Generally memories are of two types: RAM (Random Access Memory) and ROM (Read Only Memory). ROM is also called as permanent memory as it is designed once and it is used only for reading. While RAM is used for both read and write. RAM is again classified in two types: SRAM and DRAM. In this work power minimized SRAM Memory system is designed.

Power dissipation is the main constraint when it comes to Portability. The mobile device consumer demands more features and extended battery life at a lower cost. About 70% of users demand longer talk and stand-by time as primary mobile phone feature. Top 3G requirement for operators is power efficiency. Customers want smaller & sleeker mobile devices. This requires high levels of Silicon integration in advanced processes, but advanced processes have inherently higher leakage current. So there is a need to bother more on reducing leakage current to reduce power consumption.

2. PREVIOUS RELATED WORK

A trend shows that low power design techniques are becoming more important in the current industry. Considerable attention has been paid to the design of low-power for applications such as hand-held devices and wireless communications. There are numerous ways to reduce the power dissipation at the cost of area and speed. This section provides previous work that discusses low power SRAM techniques.

One of the main reasons causing the leakage power increase is increase of sub threshold leakage power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower.

In addition to Sub threshold leakage, another contributor to leakage power is gate-oxide leakage power due to the tunneling current through the gate-oxide insulator. Since gate-oxide thickness will be reduced as the technology decreases, in nanoscale technology; gate-oxide leakage power may be comparable to Sub threshold leakage power if not handled properly. However, we assume other techniques will address gate-oxide leakage; for example, high-k dielectric gate insulators may provide a solution to reduce gate-leakage Therefore, this project focuses on reducing sub threshold leakage power consumption. In this dissertation, we provide novel circuit structure named "Asymmetric Sleepy Stack" as a new idea for designers in terms of static power.

The Most well-known traditional approach is the sleep approach. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. Figure 1 shows its structure. The sleep transistors are turned on when the circuit is active and

turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively.

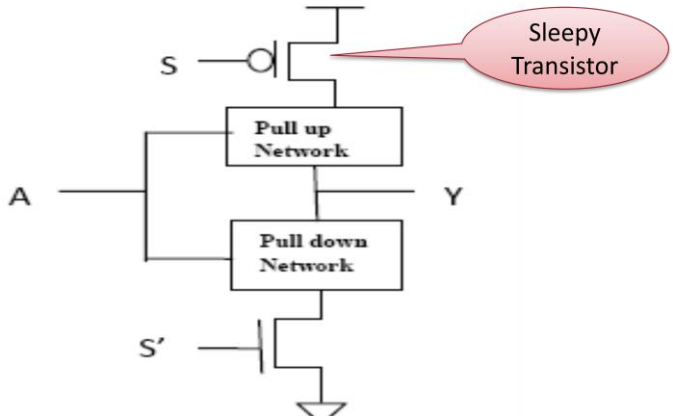


Figure 1: Sleepy method

Drawback of this technique can not retain exact logic state there for the delay is more.

When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. This takes place when more than one transistor in series is turned off. Thus the transistor stacking places the unused parts of memory in a low leakage current mode. An additional NMOS is introduced inside the leakage path. That transistor is kept on for used portion. So, there is no effect in normal operation of memory. But for the unused portion, the extra NMOS is kept off. It does not affect the normal operation of memory but reduces the amount of leakage current to a great extent due to transistor stacking effect..

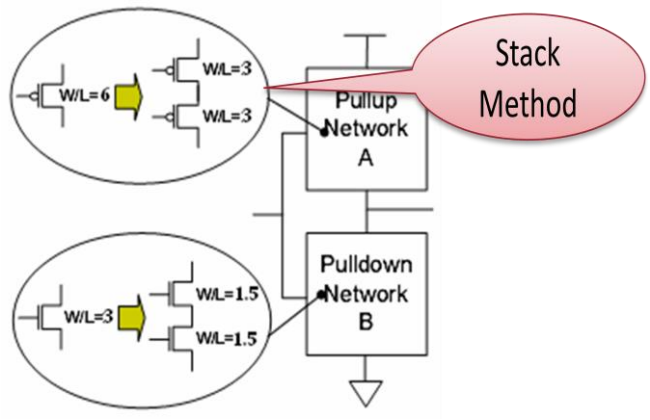


Figure 2: Stack method

In the sleepy stack structure has a combined structure of the forced stack and the sleep transistor techniques. Its combination of sleepy and stack. The forced stack inverter breaks existing transistors into two transistors and forces a stack structure to take advantage of the stack effect;

Meanwhile, the sleep transistor inverter isolates existing logic networks using sleep transistors. The stack structure saves leakage power consumption during sleep mode. This sleep transistor technique frequently uses high-Vth sleep transistors (the transistors controlled by S =1 and S' =0) to achieve larger leakage power reduction. The sleepy stack technique has a structure merging the forced stack technique and the sleep transistor technique. Figure 3 shows a sleepy stack inverter. The sleepy stack technique divides existing transistors into two transistors each typically with the same width W1 half the size of the original single transistor's width W0 (i.e., W1 = W0/2), thus maintaining equivalent input capacitance. The sleepy stack inverter in Figure 3(uses W/L = 3 for the pull-up transistors and W/L = 1.5 for the pull-down transistors, while a conventional inverter with the same input capacitance would use W/L = 6 for the pull-up.

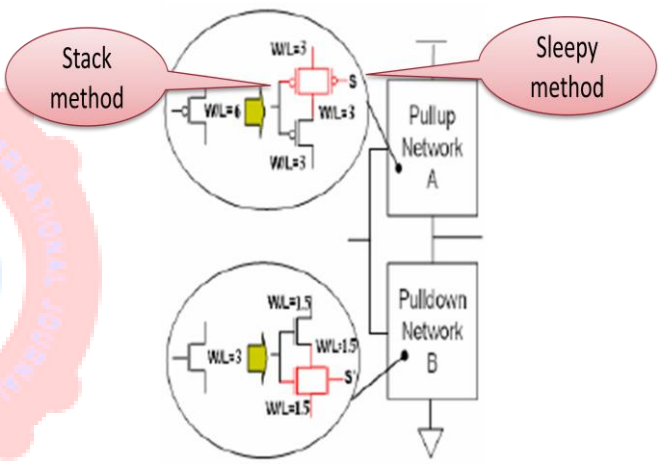


Figure 3: Sleepy Stack Method

3. DESIGNING OF ASYMMTRIC SLEEPY STACK SRAM

3.1 Conventional SRAM Cell

Fig 1 shows the conventional 6T SRAM cell. A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (P1, P2, N1, and N2) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote '0' and '1'. Two additional *access* transistors serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (WL) which controls the two *access* transistors N3 and N4 which in turn, control whether the cell should be connected to the bit lines BL and BLB (Bit Line and Bit line Bar). These bit lines (BL and BLB) are used to transfer data for both read and write operations.

3.2 Sleep Transistor Techniques

In this technique, the sleep transistors are used at two different positions. One is between the pull-up network and Vdd, then the other is between the Gnd and the pull-down network.

The size of the sleep transistor is obtained with respect to the pull-up or pull-down transistors connected to the sleep transistors

Fig. 2 shows the SRAM using the sleep transistor technique. Here the size of the pull-up or pull-down transistors are W/L=6 and W/L=3, so the size of the pMOS and nMOS sleep transistors is W/L=6 and W/L=3 respectively. High-Vth transistors are used for sleep transistors, if dual Vth values are available. while the logic circuits are not in use, the sleep transistors are turned off. By isolation of the logic networks, with the help of the sleep transistor in the sleep mode, leakage power is reduced dramatically. Moreover , the sleep transistors added additionally will increase area and delay.

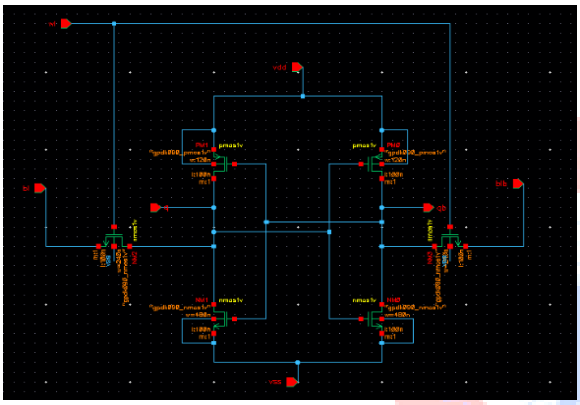


Figure 4 : Conventional SRAM Cell

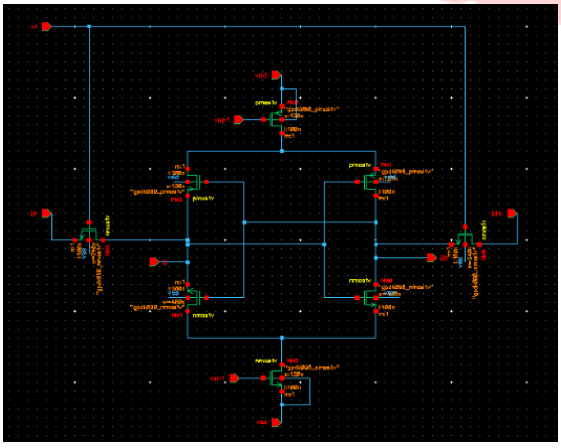


Figure 5: Sleepy technique of SRAM Cell

3.3 Sleepy Stack Techniques

Now we explain how the sleepy stack works during active mode and during sleep mode. Also, we explain leakage power saving using the sleepy stack structure. The sleep transistors of the sleepy stack operate similar to the sleep transistors used in the sleep transistor technique in which sleep transistors are turned on during active mode and turned off during sleep mode. During active mode S = 0 and ~S = 1 are asserted, and thus all sleep transistors are turned on. This sleepy stack structure can potentially reduce circuit delay in two ways. First, since the sleep transistors are always on during active mode, the sleepy stack structure achieves faster switching time than the forced stack structure; specifically, in Figure at each sleep transistor drain, the voltage value connected to the sleep transistor source is always ready and available at the sleep transistor drain, and thus current flow is immediately available to the low-Vth transistors connected to the gate output regardless of the status of each transistor in parallel to the sleep transistors.During sleep mode S = 1 and S0 = 0 are asserted, and so both of the sleep transistors are turned off. Although the sleep transistors are turned off, the sleepy stack structure maintains exact logic state. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high-Vth transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. Second, two stacked and turned off transistors induce the stack effect, which also suppresses leakage power consumption. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state.

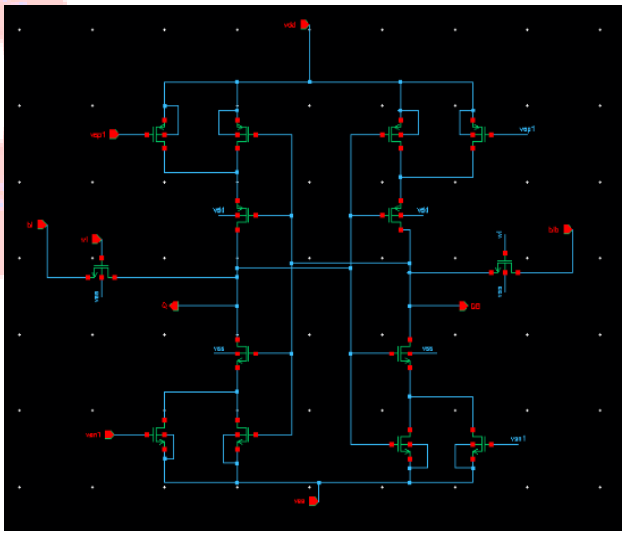


Figure 6: Sleepy Stack technique of SRAM Cell

3.4 Proposed Asymmetric Sleepy Stack Techniques

In the sleepy stack SRAM, we use Two sleepy signal one pull upside and another one in the pull down side. For combing of this two signal we require additional two more transistor totally we require 16 transistor .In the proposed Asymmetric sleepy Stack consists of one sleepy signal which is used in the pull up side and 12 transistor Which are in the required for cell design.

In Asymmetric sleepy stack power reduced by two ways

I. Sleepy method (Enabling the signal in the pull up side).
II. Stack method.

I. Sleepy method:

When sleepy signal is disabled (Vsp1=0) then circuits works in active mode and when sleepy signal is enabled (Vsp1=1) then circuit will be in standby mode cutting of power source, this technique can reduce leakage power effectively.

II. Stack method:

In the Stack method the two transistors are turned off together, which induced reverse bias between the two transistors results in sub threshold leakage current reduction. This takes place when more than one transistor in series is turned off. Thus the transistor stacking places the unused parts of memory in a low leakage current mode. An additional NMOS is introduced inside the leakage path. That transistor is kept on for used portion. So, there is no effect in normal operation of memory. But for the unused portion, the extra NMOS is kept off. It does not affect the normal operation of memory but reduces the amount of leakage current to a great extent due to transistor stacking effect.

This Asymmetric sleepy stack structure can potentially reduce circuit delay in two ways.

I. The sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode.

II. When the both sleep transistors are turned off, then also its maintains the exact logic state.

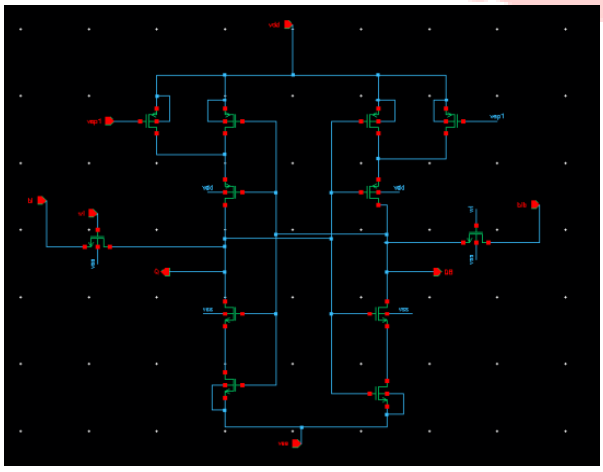


Figure 7: Proposed Asymmetric Sleepy stack SRAM Cell

4. SIMULATION AND RESULTS

The Design and Analysis are done using Cadence 90nm technology tool simulator. We compared the single cell SRAM and Asymmetric sleepy stack leakage power reduction technique with existing Sleepy Stack method, Sleepy method, Stack method and base case in terms of delay, power and area. The results shows that the sleepy stack technique is producing lesser delay, higher leakage power reduction and it also produces more stability for the circuit. We applied the sleepy stack technique in 90nm technology conventional SRAM cell and we achieved higher power reduction compared to the all low power technique. Technology and Also verified DRC,LVS,RCX for all low power SRAM cell.

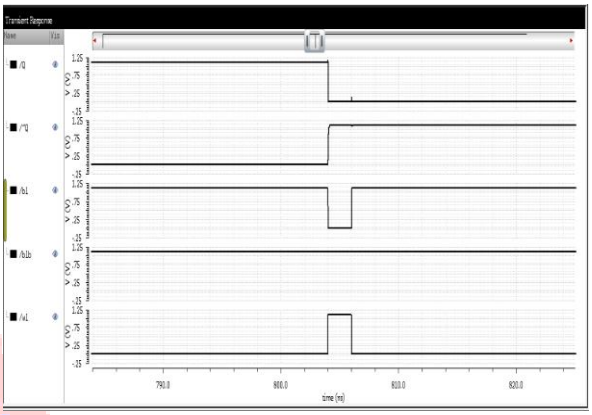


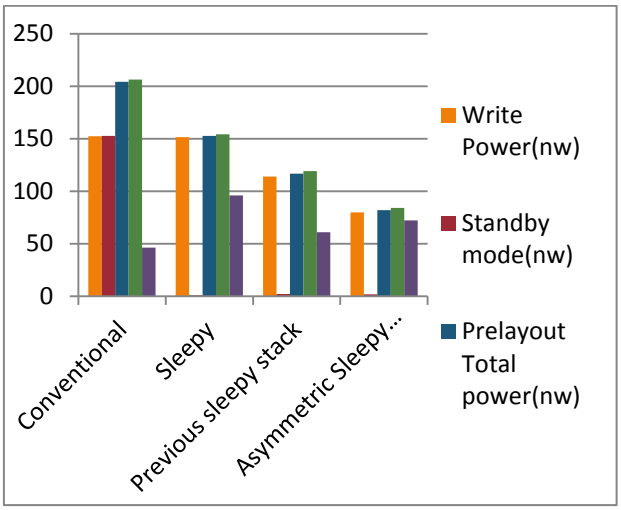
Figure 8: Output waveforms of SRAM for Write '1' and Write '0'.

- Q=1 when bl =1, blb =0, wl =1
- Q=0 when bl =0 , blb =1, wl =1

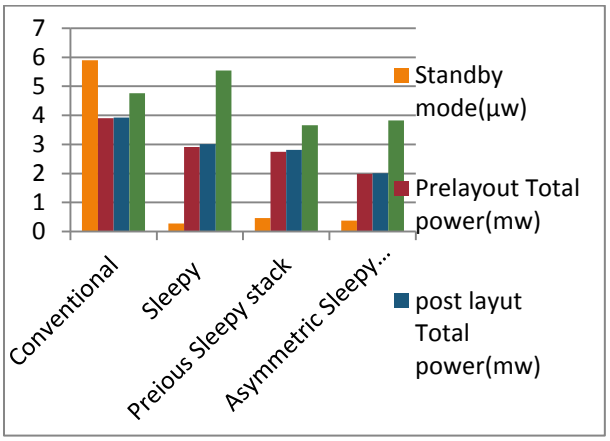
Table 1: Write power, Standby mode power, Total power, Access Time for single SRAM cell.

Single SRAM Cell	Write Power (nw)	Standby mode (nw)	Pre layout Total power (nw)	Post layout Total power (nw)	Access Time (ps)
Conventional	152.61	152.84	204.2	206.3	46.4
Sleepy	151.56	0.87	152.7	154.3	95.97
Previous Sleepy Stack	113.96	2.30	116.7	119.3	61.11
Asymmetric Sleepy stack	79.8	1.80	82.23	84.23	72.35

Graph 1: Write power, Standby mode power, Total power, Access time for single SRAM cell.



Graph 2: Standby power, Total power and Access Time for 64 bit SRAM



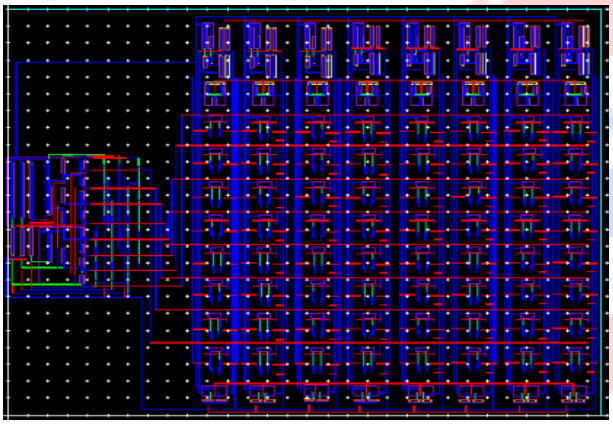


Figure 8: Layout of 64bit Asymmetric Sleepy Stack Circuit

Table 1.2: Standby power, Total power and Access Time for 64 bit SRAM

SRAM 64 bit	Standby mode (w)	Pre layout Total power (mw)	Post layout Total power (mw)	Access Time (ps)
Conventional	2.29X10^-3	3.899	3.92	476.3
Sleepy	2.726X10^-6	2.912	3.01	554.2
Previous Sleepy Stack	4.62X10^-6	2.745	2.81	365.7
Asymmetric Sleepy stack	3.8X10^-6	1.98	2.01	402.12

5. CONCLUSION & FUTURE SCOPE

Conclusion:

In this work, a Asymmetric Sleepy Stack SRAM is designed in order to reduce power dissipation with maintaining its good performance. The proposed SRAM cell consists of four additional NMOS transistors, two of which are stacked with pull down transistors of conventional 6T SRAM and other NMOS transistors are connected in feedback. The primary advantage of this SRAM is it uses same control signals as the conventional 6T SRAM, hence doesn't require any changes in the memory architecture. The high VT devices are used in shortest path in order to achieve still better performance and power reduction. The proposed SRAM is designed and simulated using *Cadence 90nm technology files*. The simulation results show that the proposed SRAM retains good logic states in read and write operations.

Further, the proposed SRAM cell is implemented in various memory systems using its supporting peripheral circuits. Various peripheral circuits such as Lyon Schediwy address decoders, 8-transistor write driver circuit, precharge circuit, high speed analogy differential 5- transistor Sense Amplifier and multiplexer are used in different configuration for different SRAM systems. The complete operation of proposed SRAM is discussed by implementing SRAM in single bit memory system. Design and simulation of high capacity SRAM systems viz., 64bit SRAM systems are also performed using appropriate peripheral circuits.

Finally, physical implementation of each of the individual peripheral circuits and proposed SRAM cell is performed using *Cadence 90nm Layout tool*. After laying out of all the circuits with no circuit violations, layout of the whole 8words X 8bits SRAM is implemented. The physical verification of the complete system is done in order make the design error free, using *DRC and LVS check*. The av-extraction of the implemented layout is done using *RCX*. The electrical properties of the presented SRAM system are analyzed and reduction of total power of the presented SRAM system is achieved through post layout simulation.

The proposed Asymmetric Sleepy Stack SRAM cell is implemented in various memory systems using its supporting peripheral circuits.

This Asymmetric Sleepy Stack SRAM cell achieves 2.5X reduction in total Power compared to conventional 6T SRAM cell and also maintains exact logic state

Future Scope:

The power dissipation and delay of the SRAM system can be still improved by using several low power and high speed peripheral circuits. The dynamic power dissipation is the dominant component of total power and it is due to large supply voltage. It can be further reduced by using low supply voltage.

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