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Power, Speed and Area analysis of 4-bit Barrel Shifter using CMOS and Pseudo-NMOS logic

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***Abstract*—Barrel shifters are widely used data path elements, integral for key computer operations like address decoding and computer arithmetic. The barrel shifter shifts data in the left or right direction by a specified number of bits. This project implements a 4 bit Mux-based barrel shifter using CMOS and Pseudo NMOS logic. The design and simulation of the same have been realized on Magic and ngSpice. A comparative analysis of various performance and characteristic parameters has been done on both logic families. This project evaluates 180 nm technology.**

I. Introduction

Barrel shifter is an essential component of the ALU and a chief component of most DSP applications. Barrel shifter is used for shifting operation like shift right logical, shift left logical, shift left arithmetic, shift right arithmetic, right rotate, left rotate. The architecture of barrel shifter can be designed by using 16 2:1 muxes (fig. 1). This project was divided in two phases. In Phase 1, the barrel shifters were implemented using CMOS and pseudo-NMOS technology on ngSpice without any parasitics. The various performance characteristics were analysed and recorded. In phase 2, the two barrel shifter layouts were optimized and implemented using 180 nm technology on Magic. The extracted spice files were then tested for area, speed and propagation delay against each other and against the outputs of phase 1. The results comprise of comparison of both logic approaches, simulations of various performance parameters, quantified effects of parasitics and optimized layouts which are helpful in low power ALU design.

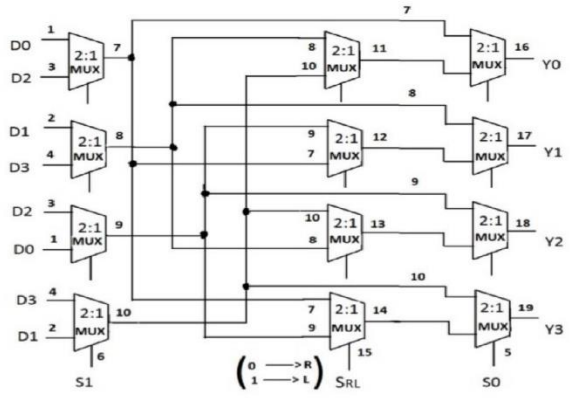


Fig. 1. 4-bit Barrel Shifter using MUXes

II. Methodology

A. CMOS 2:1 Multiplexer

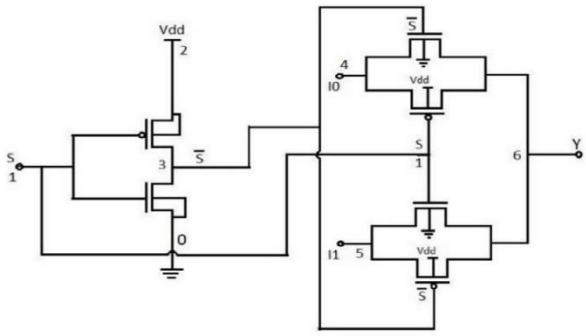


Fig. 2. Transistor level diagram of 2:1 mux using Transmission gate

The CMOS Multiplexer is made of 6 transistor. The first stage is a CMOS inverter, which takes in the select line as an input and produces its inverted version as the output. There are 2 transmission gates to which the Inputs I0 and I1 are given. The transmission gates are complementary to each other in the sense that, whenever one is active, the other is off. The upper transmission gate is active when the select line is low and the lower transmission gate is active when the select line goes high.

B. Pseudo NMOS 2:1 Multiplexer

The Pseudo NMOS logic based mux is made up of 9 transistors. The first stage is a Pseudo NMOS inverter which inverts the input select line. The drawback of this inverter are that it does not provide a perfect Vol value, has constant static power dissipation and produces relatively large propagation delay. The second stage implements the function

$$F= (S'a + Sb)'$$

where 'a' and 'b' are the inputs to the MUX with 'a' corresponding to input '0' and 'b' corresponding to input '1' . This provides an inverted output, which necessitates the Pseudo NMOS inverter in the third stage.

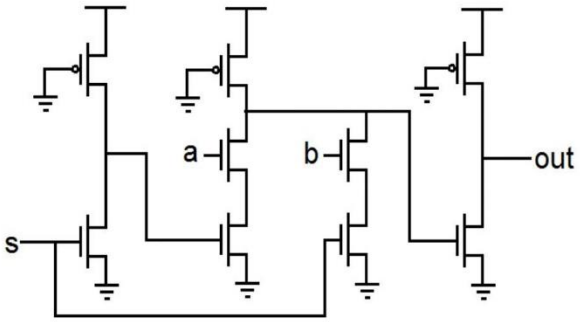


Fig. 3. 2:1 mux using pseudo NMOS logic

C. 4-bit Barrel Shifter Circuit

The aforementioned circuits for the 2:1 muxes are unit cells in the implementation of the 4 bit Barrel shifter (fig 1). The Barrel shifter has 3 modules of 4 muxes each i.e. a total of 12 muxes. Each module gets a common select input. The first and last modules have select inputs S1 and S0 respectively, which decide the amount of shift (S1 being the MSB and S0 being the LSB). The middle module has the select input SRL which decides the direction of shift with SRL =0 corresponding to a right shift and SRL =1 corresponding to a left shift.

D. ngSpice

In the first stage of this project, a Spice simulation of the 4 bit barrel shifter was done for the 2 different logic types. The Spice simulation implements the barrel shifter without considering the parasitic capacitances which may be present. A comparative study and analysis was performed on both barrel shifters. The rise time, fall time and propagation delay analysis were done and the results were recorded. Power analysis was performed on both CMOS and Pseudo NMOS muxes.

E. Magic

The second stage of the project involved creating a layout of the Barrel Shifter on Magic, so that effects like parasitics could be studied. Initially, the layout was created only for the CMOS based 2:1 Mux and Pseudo NMOS 2:1 Mux. The layouts for these were optimized so as to minimize area and routing length. The optimized muxes were then used as the basic standard component for implementation of the larger barrel shifter. Various factors such as minimum poly area and minimum transistor sizing were considered while performing this task. Power Rings were created around the cell. After completion of the layout, the circuit was extracted into Spice and an analysis similar to one mentioned above was carried out. These circuits included parasitics and gave different results compared to the basic ngSpice simulations.

III. Analysis and Results

A. Functionality check

An input data 1101 is applied to the barrel shifter keeping the select lines S1= 0 and S0= 1 and Srl= 0.
The Select line S0 is switched from 1 to 0. The Barrel Shifters should theoretically provide a single right shift i.e. give 1110 as the output initially and then provide a zero shift when the select line is switched to zero i.e. give 1101 as the output. The Barrel Shifter outputs from both the ngSpice simulations and the extracted layout matched these expected results and the following graphs were obtained.

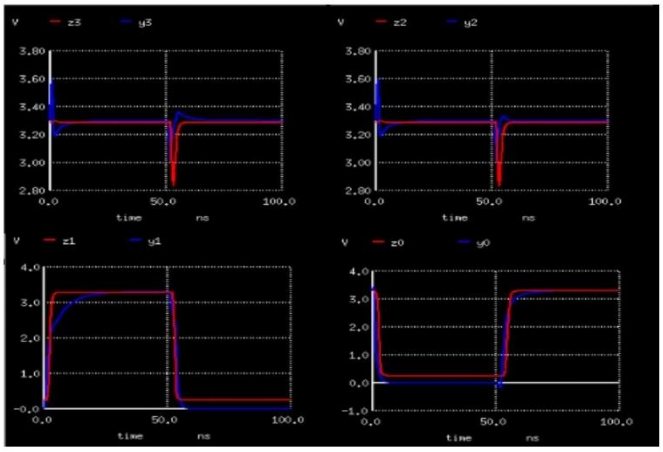


Fig. 4. The red line corresponds to the Pseudo NMOS based Barrel Shifter and the blue line corresponds to the CMOS Barrel Shifter

This analysis confirms the functionality of the Barrel Shifter, and provides an indication about the imperfect Vol level in case of the Pseudo NMOS Barrel Shifter (0.25 V instead of ideal 0 V).

B. Rise time, Fall time, Propagation delay and Voh-Vol Comparison

A pulse train is applied to the select line input S of the 2:1 Multiplexer and the corresponding outputs of both the Pseudo NMOS and CMOS Mux were plotted against each other. The following graphs were obtained when the inputs at the 2 terminals of the MUX are given as 0 and 3.3 V (Corresponding to input 0 and input 1).

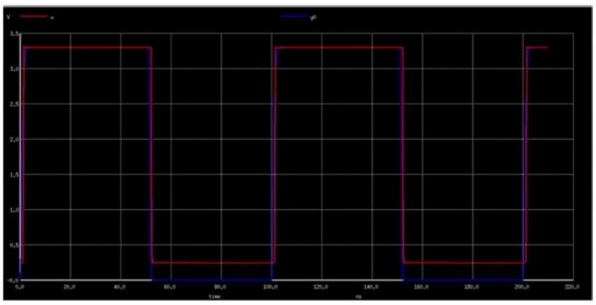


Fig. 5. This graph shows output obtained when analysis is performed on a circuit without parasitics on ngSpice.

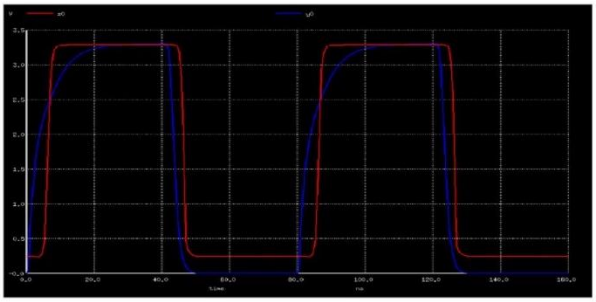


Fig. 6. This graph shows output obtained when analysis is performed the circuit extracted from the MAGIC layout including parasitics.

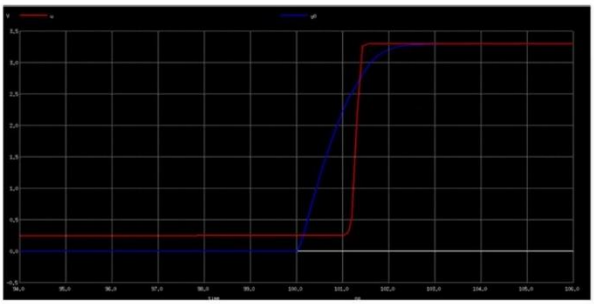


Fig. 7. Rise time comparison

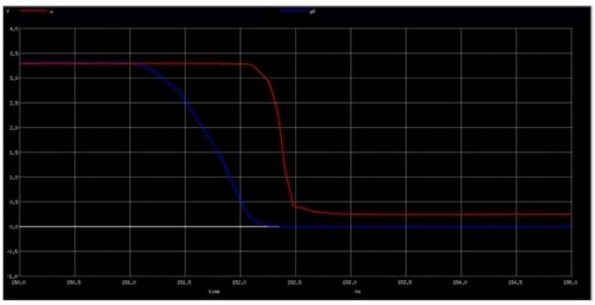


Fig. 8. Fall time comparison

The red line corresponds to the output Pseudo NMOS mux and the blue line corresponds to the output of the CMOS mux. Both Graphs show that the Pseudo NMOS while having a larger propagation delay shows quicker rise time and fall time. The increase in the propagation delay for the Pseudo NMOS mux can be attributed to the final additional inverting stage.

In both the cases, the Pseudo NMOS mux does not provide a perfect Vol value. It is 0.25 V which is far greater than the ideal 0 V. Secondly, the Magic extracted circuit shows higher rise time and fall time owing to presence of parasitics.

C. Static and Dynamic Power dissipation

The following graphs show the dynamic power dissipation in the CMOS and Pseudo NMOS multiplexers, when a pulse train is applied to the select input.

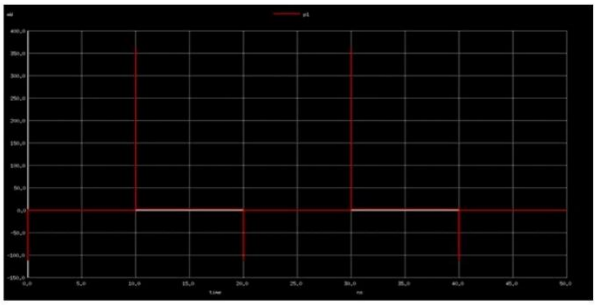


Fig. 9. Power dissipation in CMOS MUX without parasitics analysed using ngSpice

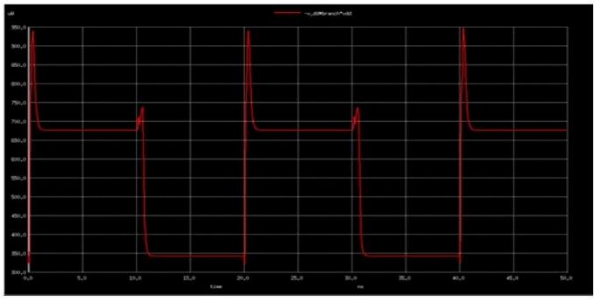


Fig. 10. Power dissipation in Pseudo NMOS Mux without parasitics

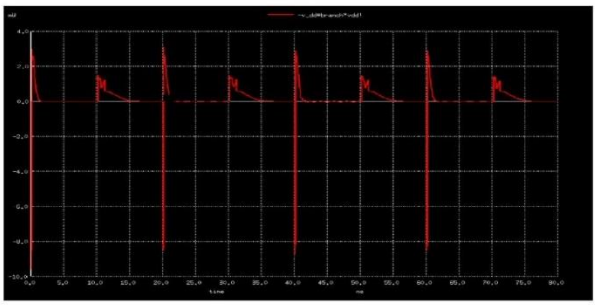


Fig. 11. Power dissipation in extracted CMOS mux

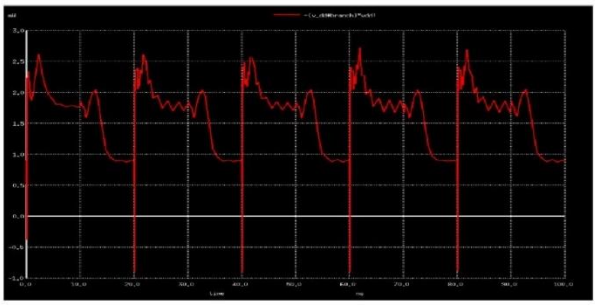


Fig. 12. Power dissipation in extracted Pseudo NMOS mux

The CMOS mux does not show static power dissipation. It dissipates power only during transitions of the select line input. The Pseudo NMOS mux shows significant static power dissipation, as the pull up does not go into cutoff when the pull down is on. The power dissipation in both logic significantly

increases in the presence of parasitics. The various spikes seen in graphs of extracted muxes, are due to charging and discharging cycles of various parasitic capacitances.

D. Effects of Parasitics

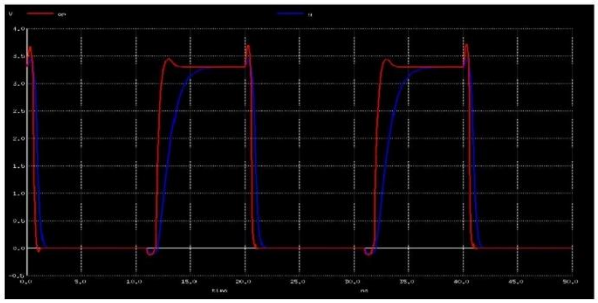


Fig. 13. CMOS logic

The red line indicates the ngSpice circuit output in the absence of parasitics. The blue line indicates the extracted circuit output considering parasitics.

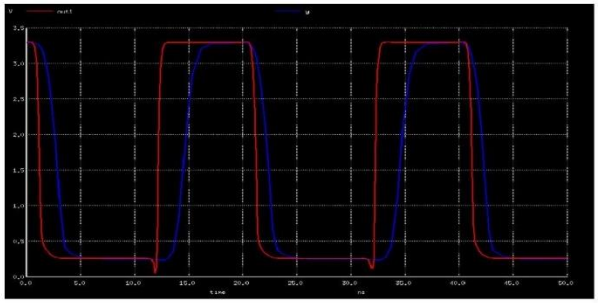


Fig. 14. Pseudo NMOS logic

The presence of parasitics increases the rise time and fall time and leads to a higher propagation delay.

IV. MAGIC LAYOUT

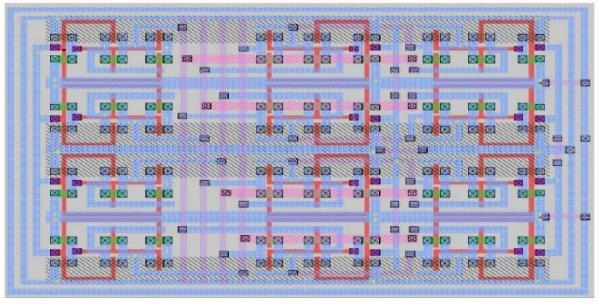


Fig. 15. CMOS based 4-bit Barrel Shifter

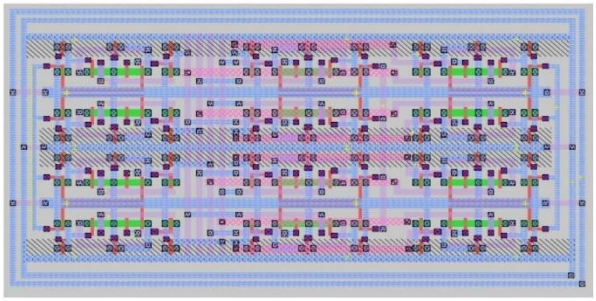
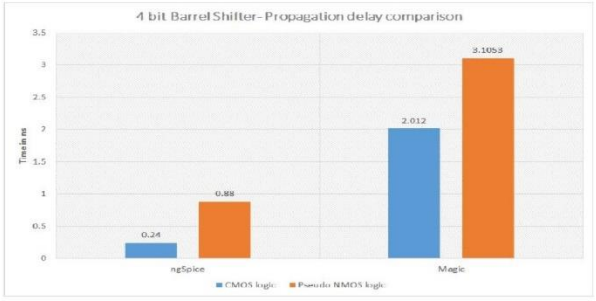


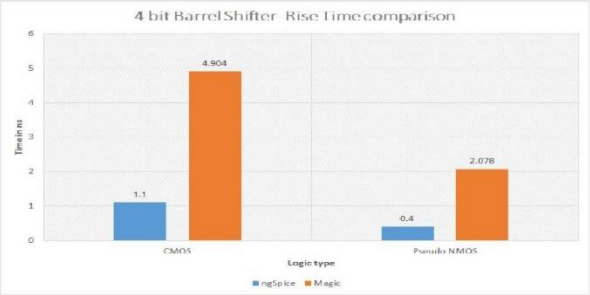
Fig. 16. Pseudo NMOS based 4-bit Barrel Shifter

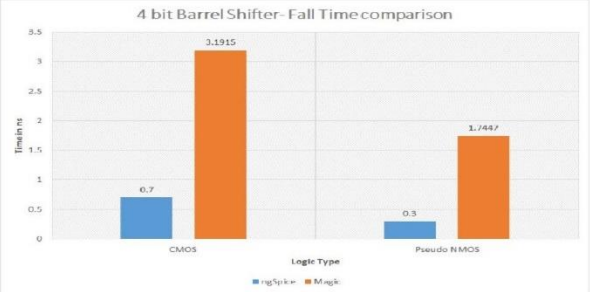
V. CONCLUSION

	CMOS (Magic)	Pseudo NMOS (Magic)	CMOS (Ngspice)	Pseudo NMOS (Ngspice)
Propagation Delay	Lower (2.012 ns)	Higher (3.1053 ns)	Lower (0.24 ns)	Higher (0.88ns)
Rise Time	4.904 ns	2.078ns	1.1ns	0.4ns
Fall Time	3.1915 ns	1.7447 ns	0.7ns	0.3ns
Max Power	3mW	2.5mW	0.58mW	0.95mW
No Of Transistors	72	108	72	108
VOL	0 V	0.232 V	0	0.248 V

In this project a 4 bit barrel shifter was implemented using Pseudo NMOS and CMOS Logic design approaches. The Pseudo NMOS Barrel Shifter used 108 transistors compared to the 72 transistors used in the CMOS Barrel Shifter. ngSpice Simulations of these Barrel Shifters showed that CMOS based design has a lower propogation delay while having rise time and fall time .It was observed that the Pseudo NMOS based Barrel Shifter has a continuous power dissipation due to a non zero Vol. The circuit was optimized and implemented on MAGIC using 180nm technology so as to minimize area and power consumed. The layout was then extracted and analyzed on ngSpice so as to yield insight into the effect of parasitics on these circuits. The results of these analysis, were in agreement with the initial results except for the higher rise time, fall time, power and propagation delay due to parasitic capacitances.
In conclusion, even though CMOS technology has a higher rise time and fall time, it is preferred over the Pseudo NMOS technology due to its lower area, lesser power consumption and minimal propagation delay.







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