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LOW DATA RATE BPSK DEMODULATION IN PRESENCE OF DOPPLER

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***Abstract* : The carrier signals received from LEO satellites invariably will exhibit Doppler shift in the carrier frequency. If the carrier is BPSK modulated with data of bit rate comparable to or less than the Doppler frequency, conventional Costas loop demodulators fail to demodulate the signal. This paper presents a configuration developed for demodulating BPSK modulated S-band carrier received from a LEO satellite. The technique is developed for extracting 20 KBPS data from the BPSK modulated signal received from a student satellite -PISAT being developed at PES Institute of Technology, Bangalore. The concept is verified with MATLAB simulation carried out for a data of 100 BPS modulating a carrier of 100 KHz. Doppler frequency of 1 KHz is considered for simulation. The system is realized on FPGA using Quartus 3 13.1 VHDL language. The design details and test results are presented in the paper**.

***Keywords* —Doppler Effect, Carrier, Quartus III 13.1.**

Introduction

The range of 2.2 to 2.3 GHz frequency range of the S-band is allotted for space to earth TTC and data transmission applications. Generally, the payload digital data is transmitted using BPSK or QPSK modulation based on the data rate. The received S-band carrier from LEO satellites will be affected by Doppler shift.

On reception of the modulated signal at ground station, the signal is down converted to Inter Mediate (IF) frequency and then Costas loop demodulators are used conventionally to extract the data. The performance will be quite good when data rate is higher than Doppler shift. PES Institute of Technology is developing a student satellite named PISAT to be deployed into 600 km orbit, where S-band is used for transmitting payload data of the order of 20 KBPS with BPSK modulation. The Doppler shift will be as high as +/- 50 KHz in the received S-band carrier. When the data rate is comparable to or less than Doppler shift, like 20 KBPS data versus ± 50 KHz Doppler frequency in case of PISAT, the demodulation process does not yield satisfactory performance. Carrier synchronization is not possible when low data rate is modulated on the carrier and higher shift in carrier frequency is envisaged. This paper presents a configuration for extracting low data from the BPSK modulated carrier in the presence of higher Doppler shift.

I. DESCRIPTION

Conventional Costas loop demodulator [1], has an I channel and a Q channel driven by a VCO. The VCO frequency is set by the sum of the outputs from the I and Q channel detectors, which steers the VCO phase such that the I channel is in phase with the signal. The I channel output is then ideally a zero ISI wave which can be integrated and sampled to recover the data. In the presence of Doppler effect, I and Q channel outputs will have variation in frequency over the data and VCO cannot be stably controlled in the loop. If the carrier containing Doppler shift is recovered, then the data can be extracted by product multiplication of incoming modulated signal with recovered carrier not having Doppler shift. The simple schematic for obtaining data from the Doppler affected BPSK signal is shown in fig.1. Proper demodulation of the BPSK signal requires a locally generated signal which is in phase with the incoming signal carrier.

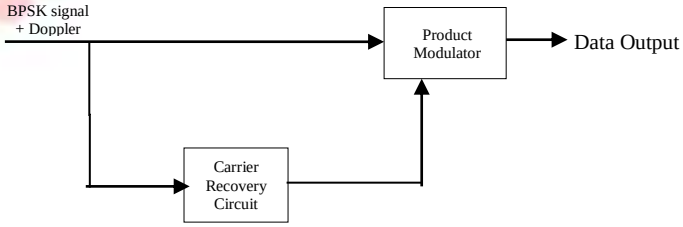


Fig. 1. **Schematic of BPSK Demodulator.**

Doppler affected carrier is recovered by using squaring loop. Fig.2 shows the configuration of carrier recovery technique using squaring loop concept.

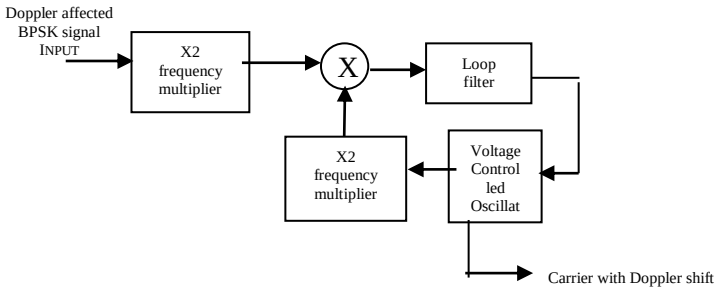


Fig. 2. **Schematic of Carrier recovery circuit.**

II. DESIGN DESCRIPTION

A.TRANSMITTER DESIGN

The transmitter mainly consists of 3 Blocks: The PN sequence Generator, The Doppler Circuit and the product Modulator.

The correlation properties of the pseudorandom noise (PN) sequence are very important in determining the Doppler. The transmitter basically consists of PN sequence generator and the Doppler circuit. An MLS-generating system can be expressed using the following recursive relation:

$$a_k[n+1] = \begin{cases} a_0[n] + a_1[n], & k = 3 \\ a_{k+1}[n], & \text{otherwise} \end{cases}$$

Where *n* is the time index, *k* is the bit register position, and ⊕represents modulo-2 addition. The data rate is given by 100 bps. The VCO generated frequency is given by 200 Hz typically characteristic where the Doppler shifted wave according to LEO satellite standards has the range given by around ±50 Khz.

The generated MLS for the entire circuit design is given by

$$p(x) = x^6 + x^5 + 1 \qquad (1)$$

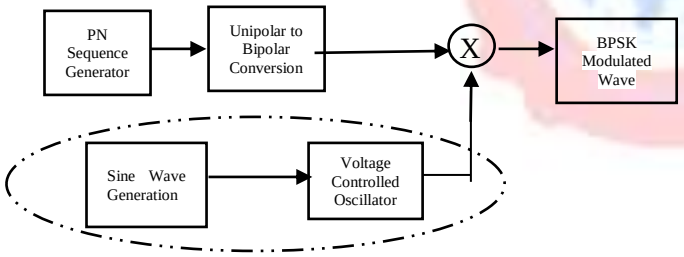


Fig. 3. **Transmitter Circuit**

B. RECEIVER DESIGN

The receiver block typically consists of the blocks that are involved in the demodulation process of the BPSK generated signal. The signal contains Doppler frequencies and the carrier is tracked using the phase locked loop. There are typically two types of demodulating techniques as will be discussed. In particular, two new techniques are developed. The first technique which is referred to as the squaring loop technique, is based on the idea of applying a linearly doubled frequency sweep to the received signal as a method to reduce the

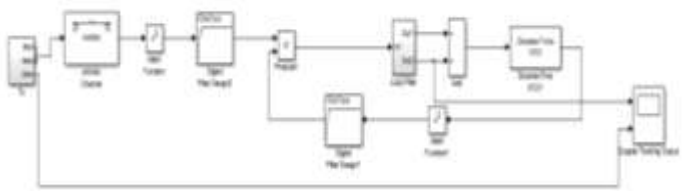


Fig. 4. **Receiver Circuit**

Doppler shift to tolerable levels, whereby conventional carrier synchronization may be employed. This method has been shown to be better suited when compared to the other conventional techniques where however, for direct overhead satellite pass, improved Doppler compensation is achieved by utilizing the modified novel technique.

Simulations have been carried out to explore the performance of the squaring loop technique and results have shown that it is capable of extracting the carrier with minimized noise in the channel as the phases between the input and output are the same.

The second technique of carrier extraction is based on the conventional Costas loop, here the carrier and Doppler is given to the loop, where the loop has the noise which produces the jitters when the carrier plus the Doppler is given, thus has the drawback, which puts a restriction on extracting the Doppler and the carrier.

The main overview is the Carrier Extraction which is obtained by the above first method, where the squaring loop is the demodulation circuit. In the design, the current circuit of study is the one with the Doppler tracked, where the noise is completely eliminated and thus gives the same phase as compared to the input signal. It is a technique used in coherent Detection of modulated signals in the receiver.

The incoming modulated signal is squared and high pass filtered to extract the carrier component at twice its original frequency. This high pass filtered signal is then conditioned further and fed into a phase locked loop whose other input comes from a VCO (Voltage Controlled Oscillator), after doubling its frequency and high pass filtering it. The error output of the phase locked loop is converted into a DC voltage which is fed back into the VCO to cause it to oscillate at a frequency which is same as the carrier frequency such that the error output reduces to zero.

The equation of VCO output is as follows where the amplitude will change the output frequency, that is, the control voltage is directly proportional to the frequency change.

$$A^* \cos (2 * \pi (f + kvco*v)t + \varphi)) \qquad (2)$$

Where kvco = The sensitivity of the Voltage Controlled Oscillator (VCO), f =The frequency of the output wave; φ = phase difference of the output wave as compared to the input wave.

III. FILTER DESIGN

The filter designed in our model is a high pass filter with the pass band frequency of around 50000 Hz. The filter typically designed involves the use of the elliptical filter and the IIR types based on the impulse response.

The sampling frequency for the filter implemented has the value of 8000000 Hz. The study of various response of the magnitude and phase response, power and frequency plot and the pole zero plot has been implemented.

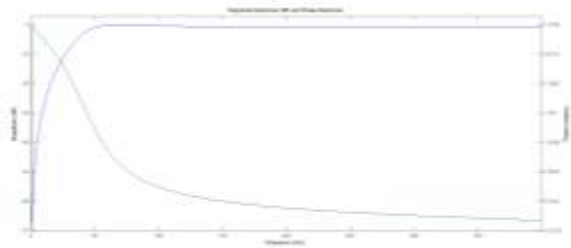
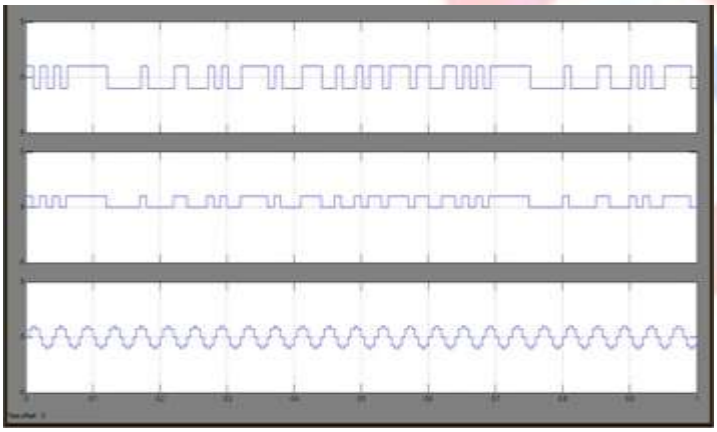


Fig. 5. **Magnitude and Phase Plot**

The implementation of the filter is done using the direct form-I realization.

The following simulation result depicts the demodulated output when the data rate given at the input is 100 bps. The above graph represents the very fact that the PN sequence is obtained or reflected in the output is because the Doppler signal (sine signal) follows the integrator path output. The sine signal following the integrator path output also signifies the tracking of carrier.

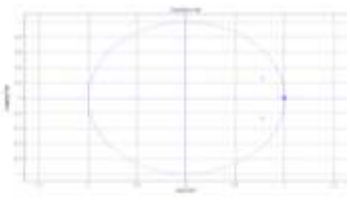


. Fig .6. **Output with input modulated wave**

The Doppler and carrier is separated using the squaring loop where the input PN sequence is reflected at the output when recovered using the product modulator where the VCO output is tapped with the output of the modulator to give the output.

The output is verified through Matlab simulations.

$$H(s) = \frac{K_d K_o (s\tau_2 + 1)/\tau_1}{s^2 + s K_d K_o \tau_2/\tau_1 + K_d K_o/\tau_1}$$



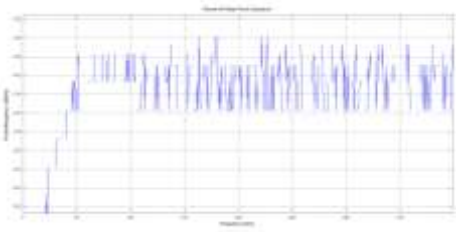


Fig. 7. **Pole Zero Diagram**

The PLL frequency phase offset is observed with the Doppler frequency being replaced by a constant input DC voltage given to the VCO. The simulations for the resulting circuit diagram is observed in MATLAB.

The figure 8 typically represents the damping factor variations which denotes the extent of locking of the PLL circuit. Natural frequency and damping factor are an attractive set of parameters because of their intuitive physical description and because of their widespread occurrence in the PLL literature. Strictly speaking, though, they apply only to second-order loops.

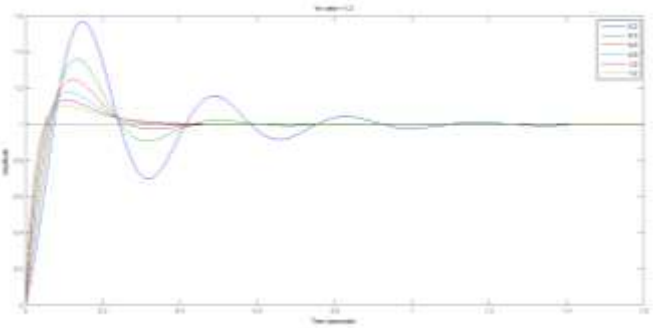


Fig. 7. **Damping Factor Variations**

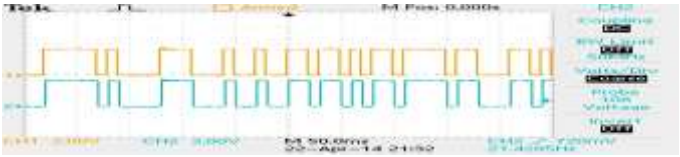
An extended definition of damping factor is feasible for type 2 loops of higher than second order but the concept becomes meaningless for a first-order PLL or for a PLL of type 3 or larger.

Values of τtypically lie between 0.5 and 2, with 0.707 often a preferred value, but much larger values-up to 20 or 30-are sometimes needed. Loops with damping smaller than ~0.5 have excessive overshoot in their transient responses are dynamically unsatisfactory. The figure 8 typically gives an idea about the variation of zeta as the locking of the same is with respect to the PLL.

The PLL has different locking range for different values of zeta as illustrated in the diagram; it takes more time to lock for lower values of zeta and vice versa.

IV. BER PERFORMANCE

In this paper, typically the BER rate is studied with the variation of the error rate with the Eb/No performance. The variations are plotted and tabulated with the ideal value, being



10 for the BPSK signal. The probability of error calculated is a

bell shaped curve with the center denoting the ideal value for any system. The BER performance is obtained by comparing the demodulated signal with the input data sequence. The PN sequence data in our case is typically sent at 100bps. The data transmitted is checked for the corresponding bit errors when the rising edge corresponds to the rising edge and the falling edge corresponds to the falling edge in the demodulated output. The entire performance is simulated by adding the sample and hold block, with demodulated output and input data sequence as the inputs to the block, performing the above mentioned operations. The values tabulated for the above BER variation is also shown below with the graphical variation.

$$\text{BER} = \frac{Number\ Of\ Errors}{Total\ Number\ Of\ Bits\ Sent}$$

If the medium between the transmitter and receiver is good and the signal to noise ratio is high, then the bit error rate will be very small - possibly insignificant and having no noticeable effect on the overall system. However if noise can be detected, then there is chance that the bit error rate will need to be considered. The main reasons for the degradation of a data channel and the corresponding bit error rate, BER is noise and changes to the propagation path (where radio signal paths are used).

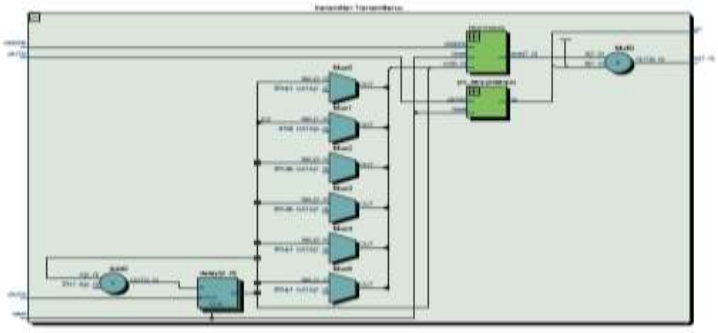
When the LEO satellite is at the Zenith, the BER will be maximum. With the decrease in orbital height, the BER for the corresponding movement increases and vice versa.

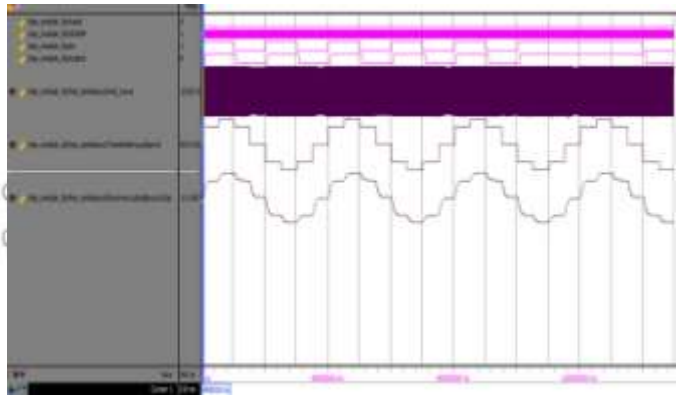
V. HARDWARE IMPLEMENTATION

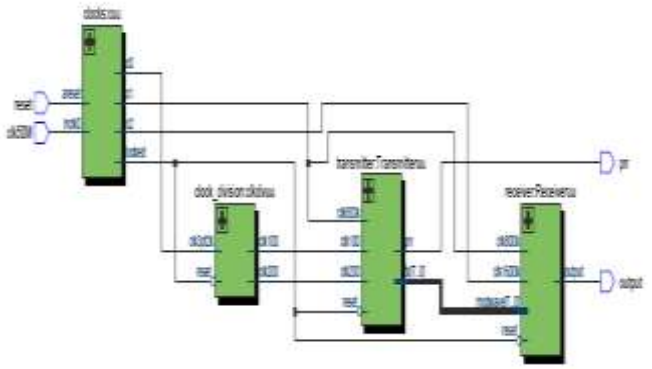
The entire model simulated using MATLAB is implemented in hardware with the signals using fixed data bits. The following model has been simulated and tested in hardware using the VHDL language and the following results have been observed.

The FPGA board (DE0 Nano) generates a clock of 50 MHz frequency. We require clock frequencies of 200 Hz, 800 kHz and 1600 kHz as sampling frequencies for the various blocks. The in-built PLL of the board is utilized to derive the required clock frequencies. While the locking of the outputs of the PLLs are in progress, the signals are not used to synchronize any further operations.

Once they are locked, they are fed as sampling frequencies to the appropriate blocks. The minimum clock frequency that can be generated in the above said manner is 2 kHz. To generate 200 Hz clock, a 3.2 kHz clock is consecutively divided 5 times, using T Flip Flop in each step.







The input PN sequence is typically generated using the delay blocks. The VCO (voltage controlled oscillator) is implemented by generating an equivalent NCO (numerically controlled oscillator). LUTs (Look up Tables) are used.

VI. RESULTS AND CONCLUSIONS

The relative motion between the transmitter and the receiver will cause a shift in frequency, thus making the tracking of actual frequency difficult. This paper, illustrates with the experimentation and the observed results, showing that the use of the tracking circuits like the squaring loop, where PLL is used for the locking of the carrier. The concept has been verified for the demodulator output where the BER performance is also observed. The entire circuit has the different Doppler frequencies verified with the concept of the Doppler tracking till now. The frequency of the signals transmitted from Low Earth Orbiting (LEO) satellites will be effected by Doppler shift. Demodulating low bit rate data in the presence of Doppler shift becomes extremely difficult with conventional methods that use Costa's loop architectures.

This paper has presented the configuration developed for demodulating BPSK modulated carrier and extract data in the presence of high Doppler shift. The carrier having Doppler shift is extracted first by using squaring loop technique.

Generated carrier is used for demodulating the received IF signal for extracting the data. The configuration has been arrived by simulating on MATLAB. For simulation, Data at

bit rate of 100 BPS is BPSK modulated on a 100 KHz carrier and 1KHz Doppler is added to the carrier. BER performance is also verified in simulation. Finally, the system has been realized on FPGA using Quartus 3 13.1 VHDL language. The hardware is tested and the results have been presented in the paper. The following project can be converted to RF and can be used for further development. The real time applications include the LEO satellite and the radar.

The following signifies the output where the sine signal tracks the K2 output thus reflecting the tracking of the carrier. The Doppler and carrier is separated using the squaring loop where the input PN sequence is reflected at the output when recovered using the product modulator where the VCO output is tapped with the output of the modulator to give the output.

From the above results, it can be seen that for different Doppler frequencies can be tracked and the demodulated data can be used for further analysis. From the observed results the bit error rate has an ideal response for the Eb/N0 value of ~10 which is the standard for BPSK. The AWGN channel included in the model will result in the bit error thus showing the deviation as per the simulation.

The BER performance is studied for various values of SNR or Eb/No. The value for which the BER performance varies entirely depends upon the extent to which the errors result in the BPSK signals. The BER performance entirely varies a function of the modulated signal. The following table typically represents the variation of the BPSK signal with Eb/N0. The entire variation is sketched with a written MATLAB code.

VII. ACKNOWLEDGEMENT

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