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XOR Gate Design Using Reversible Logic in QCA and Verilog Code

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***ABSTRACT:*Quantum Cellular Automata also known as QCA, deals with Quantum Dots which are semiconductor particles whose size ranges in nanometers, hence the name nanotechnology. Quantum cellular automata is an emerging nanotech which is speed, small in size and minimum power consumption compared to CMOS technology. In QCA, binary information is encoded as electronic charge configuration of a cell. Fundamental unit in building of QCA circuit is a QCA cell. A QCA cell is an elementary building block which can be used to build basic gates and logic devices in QCA architecture [1]. In this paper we are going to implement XOR GATE using basic gates like AND, OR and NOT gates in QCA. Also, we are calculation the total area occupied by the circuit and power dissipated by that circuit. Using this implemented circuit, we are comparing the Verilog coded design of XOR GATE in terms of area and power dissipated.**

Keywords: CMOS, QCA (Quantum Cellular Automata), XOR Gate, Verilog HDL.

1. INTRODUCTION

VLSI technology has progressed remarkably. However, these progresses may slowdown in future. Among the chief technological limitations for this slowdown are the interconnect problem and power dissipation. As more and more devices are packed into the same area, the heat generated during a switching cycle can no longer be removed and may result in damage to the chip[1].

On the other hand, QCA provides an alternative technology to reduce the power dissipated in a circuit. QCA has high speed of execution, parallel processing and has reduced power dissipation than compared to any other devices. These kind of advantages in QCA Design makes it more useful than other designs. On the other hand, when we compare it with Verilog HDL coding, the length of the code for a design or circuit might be more and there are main modules and test benches which makes the code very lengthy. Verilog code execution has more number of steps like synthesis, check syntax, behavioral execution and simulation. So, it makes the step more length and time consuming and if we fail in any step during execution, the result may not be obtained. Where as in QCA, area occupied is less and execution is fast with one step and by providing proper clocking, the noise or error in the output is reduced.

XOR GATES specially used as the basic difference detector. The truth table of XOR GATE says, if both the inputs are same, the output is active low i.e., logic ‘0’ and if the input are different then the output is active high i.e., logic ‘1’.

Power dissipation can be reduced by minimizing the circuit area. This area depends on the number of cells occupied by the circuit.

If the circuit has less number of cells, area of the circuit is reduced, in turn power dissipation is reduced. This is the main advantage of QCA Design when compared to other hardware or software design.

2. QUANTUM CELLULAR AUTOMATA

QCA or Quantum Cellular Automata can be of 2 types. This classification is based on the dots arranged inside the Quantum cell. First type of QCA cell consist of the quantum dots at the corners of the square. The second type is just similar to the first one, but they have their cells arranged at the middle of each side. There is one force which involves in transferring the data or movement of electrons between the cells known as coulomb repulsion, where the electrons always move or occupy in diagonally opposite dots.

2.1. QCA Cell

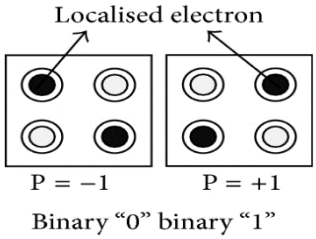

Figure 1. Cell Representation

In the above diagram, we can see both types of Quantum cells. In our regular basis we use the first type of cells where the Quantum Dots are arranged at the corners of the cells. The electrons are arranged in the diagonal order as shown in the figure 1.

The cell has two types of polarizations, which is nothing but the arrangement of electrons in the diagonal dots. If the electrons are arranged as shown in first QCA cell, then it is polarization is +1, if opposite, then it is -1. Polarization +1 indicates that the cell is carrying binary value 1, if the polarization is -1, then the cell is carrying binary value 0.

Before knowing about polarization in depth, we must learn about majority gates.

QCA cells can be defined as shown above. If the cell is blue in colour, then the cell is defined as input. Similarly, for output it is yellow and we have green, pink, light blue and white colours for cell clock/zone 0, clock/zone 1, clock/zone 2, clock/zone 3 respectively.

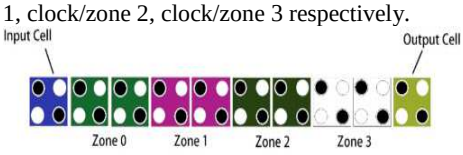

Figure 2. Cell Types

2.2. Majority Gate

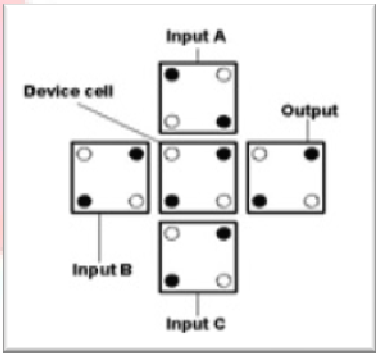

Figure 3. Majority Gate

Majority gates are the fundamental blocks of QCA which is used to build all kind of basic gates like AND and OR Gates. Majority gate basically consist of 5 QCA cells, which are arranged as shown in above figure 3 (one at the center followed by 4 cells surrounding it). Among 4 cells, three are made as inputs (which are in blue) and one is made as output (which is in yellow). The middle cell is made as device cell.

To form the basic gates, we use polarization. One among the 3 input cells in majority gate is used to give polarization input. If the polarization is -1, then the majority gate acts as

AND GATE, else if the polarization is +1, it acts as OR GATE. If we select the cell, the following window in figure 4 will open, so that we can define a cell as input/output cell or polarization cell.

The majority gate can be used as a three-input gate or just as two-input gate depending on our requirement.

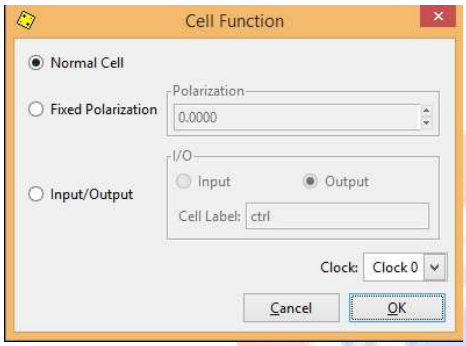

Figure 4. Cell Function block

2.3. QCA Clocking

Clocking is main step in QCA Design. Without Clocking, you may not get proper output for the give circuit. As we discussed earlier in QCA cell section, that there are four clocks in QCA and they are clock/zone 0, clock/zone 1, clock/zone 2, clock/zone 3 and each clocked cell is assigned with a particular colour.

There are 4 states in QCA Clocking and each clock represent a state in QCA as shown in fig 7. The 4 states are,

. Switch . Release

. Hold . Relax

With reference to figure 5, Clock 0 represent *switch state* where the cell which has no electrons, and which is in low state will gain electrons and get excited to higher state. Clock 1 represent *hold state* where the cell which is excited to higher state forms inter-cellular barriers and holds the excited electrons in higher state. Clock 2 represent *release state* where the inter-cellular barriers are removed, and the electrons are released. Clock 4 represent *relax state* where the excited cells will come back to lower level and the cell is free without any electrons in it. The clocking of cells should be cyclic order from input to output and it should be in same order as shown in fig below.

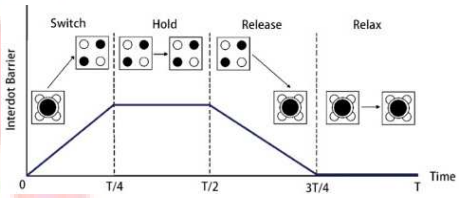

Figure 5. Clock states/cycle

3. QCA DESIGN OF XOR GATE

The main concept of this paper is to design an XOR gate using QCA Designer. XOR GATE is a digital logic gate that gives an active high or logic 1 when both the inputs are different, else it gives active low or logic 0 or we can also define as, an XOR GATE implements Exclusive-OR which gives high output when the number of high inputs is high. XOR GATE is nothing but as inequality function so, we can use XOR GATE as difference detector.

A. **Boolean equation:**

$$Y = (A \cdot \bar{B}) + (B \cdot \bar{A})$$

B. **Symbol:**

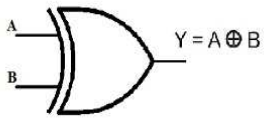

Figure 6. XOR Gate Symbol

C. **Truth table:**

Table 1. XOR Gate Truth Table

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

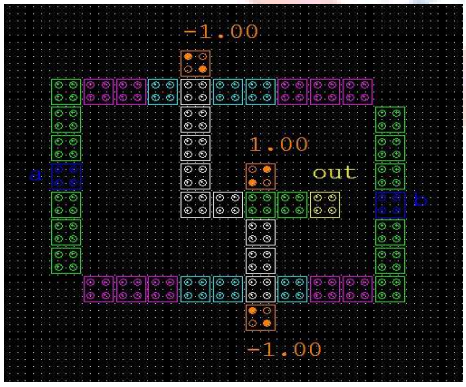

Figure 7. XOR Gate in QCA Designer

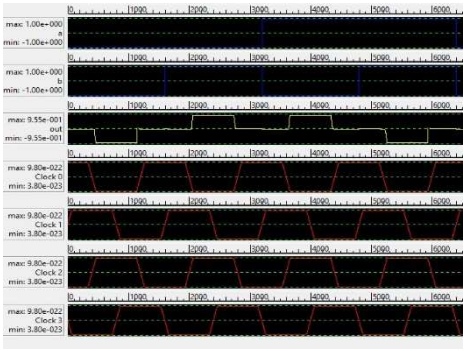

Figure 8. XOR Gate output

4. RESULT AND DISCUSSION

4.1. Area and Power Dissipation:

We already discussed in the beginning about power dissipation and area. Usually the circuits which we design requires or consumes large amount of power so, the circuits tend to generate heat. This heat should be dissipated to the surface. More amount of power is dissipated, and this kind of power wastage should be reduced, and it can be done by reducing the area occupied by the circuit. The table below gives the details of area and power calculations.

a. Power dissipation formula:

$$P_{diss} = \frac{E_{diss}}{T_{cc}} \propto \frac{h}{2Tcc}\vec{\Gamma} + \left[-\frac{\vec{\Gamma}_-}{|\vec{\Gamma}_-|}\tanh\left(\frac{h|\vec{\Gamma}_i|}{k_c T}\right) + \frac{\vec{\Gamma}_-}{|\vec{\Gamma}_-|}\left(\frac{h|\vec{\Gamma}_-|}{k_c T}\right)\right]$$

b. Comparison with References:

Table . Area and power calculation results

XOR Gate	Cell Complexity	Area(μm²)	Power Dissipation
Refer	60	0.09	-

ence [3]			
Refer ence [4]	54	0.08	-
Propo sed Circui t	45	0.06	**76.06**

4.2. Comparison with Verilog Code

Verilog code for XOR gate has main module and test bench. Main module has synthesis and check syntax and in test bench we have behavioural and simulation.

The code is mentioned below:

. Main module

```
module xorgate(
                input a, b,
                output y);

assign y=(~a)&b | a&(~b);

endmodule
```

. Test Bench

```
module testbench_xorgate();

reg a, b; wire y;

xorgate uut(.a(a), .b(b), .y(y));

initial begin

a=0; b=0; #10;

b=1; #10;

a=1; b=0; #10;

b=1; #10;

end

endmodule
```

Figure 9. Verilog Code output

5. CONCLUSION

Design of XOR GATE using QCA Designer is easy when compared to XILINX tool. Also, the area occupied, and power dissipated in QCA is less than Verilog HDL. The number of steps while executing QCA is very much low when compared to Verilog HDL.
The main advantages of XOR gate is, it is the simplest form of differentiator where if its inputs are different, the output is 1, indicating that the inputs are not alike and more over it is used in parity generator, error detector and corrector etc.

6. REFERENCES

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