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Design of an Efficient Architecture for Fault Exposure and Data Recovery for Motion Estimation Testing Applications

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***Abstract*- The critical role of motion estimation (ME) in a video coder, testing such a module is of priority concern. While focusing on the testing of ME in a video coding system, this work presents an error detection and data recovery (EDDR) design, based on the residue-and quotient (RQ) code, to embed into ME for video coding testing applications. An error in processing elements (PEs), i.e. Key components of a ME can be detected and recovered effectively by using the proposed EDDR design. Importantly, the proposed EDDR design performs satisfactorily in terms of throughput and reliability for ME testing applications. While DFT approaches enhance the testability of circuits, advances in submicron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world. BIST for the ME does not expensive test equipment, ultimately lowering test costs. Thus, extended schemes of BIST referred to as built-in self-diagnosis and built- in self-correction have been developed recently.**

Keywords –Motion estimation, error detection and data recovery, residue-and quotient code, design for testability, circuit under test.

I. INTRODUCTION

Advances in semiconductors, digital signal processing, and communication technologies have made multimedia applications more flexible and reliable. A good example is the H.264 video standard, also known as MPEG-4 Part 10 Advanced Video Coding, which is widely regarded as the next generation video compression standard Video compression is necessary in a wide range of applications to reduce the total data amount required for transmitting or storing video data. Among the coding systems, a ME is of priority concern in exploiting the temporal redundancy between successive frames, yet also the most time consuming aspect of coding. Additionally, while performing up to 60%±90% of the computations encountered in the entire coding system, a ME is widely regarded as the most computationally intensive of a video coding system. AME generally consists of PEs with a size of 4x4. However, accelerating the computation speed depends on a large PE array, especially in high-resolution devices with a large search range such as HDTV.

Additionally, the visual quality and peak signal-to-noise ratio (PSNR) at a given bit rate are influenced if an error occurred in ME process. A testable design is thus increasingly important to ensure the reliability of numerous PEs in a ME. Moreover, although the advance of VLSI technologies facilitate the integration of a large number of PEs of a ME into a chip, the logic-per-pin ratio is subsequently increased, thus decreasing significantly the efficiency of logic testing on the chip. As a commercial chip, it is absolutely necessary for the ME to introduce design for testability (DFT) DFT focuses on increasing the ease of device testing, thus guaranteeing high reliability of a system. DFT methods rely on reconfiguration of a circuit under test (CUT) to

improve testability. While DFT approaches enhance the testability of circuits, advances in sub-micron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world.

DISADVANTAGES OF EXISTING:

- Poor performance in terms of high accuracy design for real time applications in DCT core on FPGA implementation.
- Does not achieve in terms of implementation on CMOS technology DCT core.

ADVANTAGES OF PROPOSED:

- To fit for Real Time application in DCT Core.

II. PROPOSED SYSTEM

The conceptual view of the proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) in Fig. utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors.

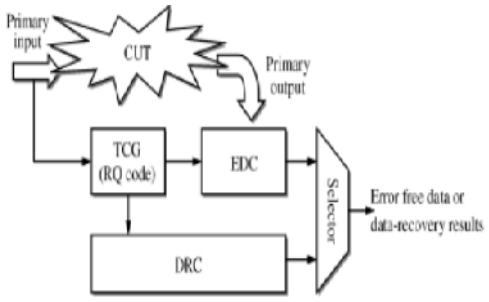

Fig.1. Proposed EDDR architecture.

DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDDR scheme to detect errors and recover the corresponding data.

III. RQCODEGENERATION

Coding approaches such as parity code, Berger code, and residue code have been considered for design applications to detect circuit errors[3],[4]. Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. Error detection logic for operations is typically derived by a separate residue code, making the detection logic is simple and easily implemented. For instance, assume that N denotes an integer,N_1 and N_2 represent data words, and m refers to the modulus. A separate residue code of interest is one in which N is coded as a pair (N,$|N|_m$). Notably, $|N|_m$ is the residue of N modulo m. Error detection logic for operations is typically derived using a separate residue code such that detection logic is simply and easily implemented. However, only a bit error can be detected based on the residue code. Additionally, an error cannot be recovered effectively by using the residue codes. Therefore, this work presents a quotient code, which is derived from the residue code, to assist the residue code in detecting multiple errors and recovering errors. The mathematical model of RQ code is simply described as follows. Assume that binary data X is expressed as

$$X = \{b_{n-1}b_{n-2} \ldots . b_2 b_1 b_0\} = \sum_{j=0}^{n-1}(b_j 2^j). \quad (1)$$

The RQ code of X modulo m expressed as $R = |X|_m$ $Q = X/m$, respectively. Notably i denote the largest integer not exceeding i.

According to the above RQ code expression, the corresponding circuit design of the RQCG can be realized. In order to simplify the complexity of circuit design, the implementation of the module is generally dependent on the addition operation. Additionally, based on the concept of

residue code, the following dentitions shown can be applied to generate the RQ code for circuit design.

Definition1:

$$|N_1+ N_2|_m = ||N_1|_m + |N_2|_m|_m. \quad (2)$$

Definition2: Let $N_j = n_1+n_2+\cdots+n_j$, then

$$|N_j|_m = ||n_1|_m+|n_2|_m+\cdots+|n_j|_m|_m. \quad (3)$$

To accelerate the circuit design of RQCG, the binary data shown in (1) can generally be divided into two parts:

$$X = \sum_{j=0}^{n-1}(b_j 2^j)$$

$$= \sum_{j=0}^{k-1}(b_j 2^j) \perp 2^k \sum_{j=k}^{n-1}(b_j 2^{j-k})$$

$$= Y_0 \perp Y_1 2^k$$

Significantly, the value of k is equal to [n/2] and the data formation of Y_0 and Y_1 are a decimal system. If the modulus $m = 2^k - 1$, then the residue code of X modulo m is given by

$$R = |X|_m$$

$$= |Y_0 \perp Y_1|_m$$

$$= |Z_0 \perp Z_1|_m = |Z_0 \perp Z_1|_\alpha$$

$$Q = \frac{X}{m}$$

$$= Z_1 \perp Y_1 + \beta$$

Where

$$\alpha(\beta) = \begin{cases} 0(1), & \text{if } Z_0 \perp Z_1 = m \\ 1(0), & \text{if } Z_0 \perp Z_1 < m \end{cases}$$

Notably, since the value of $Y_0 \perp Y_1$ is generally greater than that of modulus m, the equations for R and Q must be simplified further to replace the complex module operation with a simple addition operation by using the parameters Z_0, Z_1,α and β.

Based on R and Q, the corresponding circuit design of the RQCG is easily realized by using the simple adders (ADDs). Namely, the RQ code can be generated with a low complexity and little hardware cost.

IV. Fault Model

The PEs are essential building blocks and are connected regularly to construct a ME. Generally, PEs are surrounded by sets of ADDs and accumulators that determine how data flows through them. PEs can thus be considered the class of circuits called ILAs, whose testing assignment can be easily achieved by using the fault model, cell fault model (CFM) [5].Using CFM has received considerable interest due to accelerated growth in the use of high-level synthesis, as well as the parallel increase in complexity and density of integration circuits(ICs).Using CFM makes the tests independent of the adopted synthesis tool and vendor library. Arithmetic modules, like ADDs (the primary element in a PE), due to their regularity, are designed in an extremely dense configuration.

Moreover, a more comprehensive fault model, i.e. the stuck-at (SA) model, must be adopted to cover actual failures in the interconnect data bus between PEs [6].The SA fault is a well known structural fault model, which assumes that faults cause a line in the circuit to behave as if it were permanently at logic “0” (stuck-at 0 (SA0)) or logic “1” [stuck-at 1 (SA1)].The SA fault in a ME architecture can incur errors in computing SAD values. A distorted computational error (e) and the magnitude of e are assumed here to be equal to SAD'-SAD, where SAD' denotes the computed SAD value with SA faults.

V. TCG Module

According to Fig.2,TCG is an important component of the Proposed EDDR architecture. Notably, TCG design is based on

the ability of the RQCG circuit to generate corresponding test codes in order to detect errors and recover data. The specific in Fig. 2

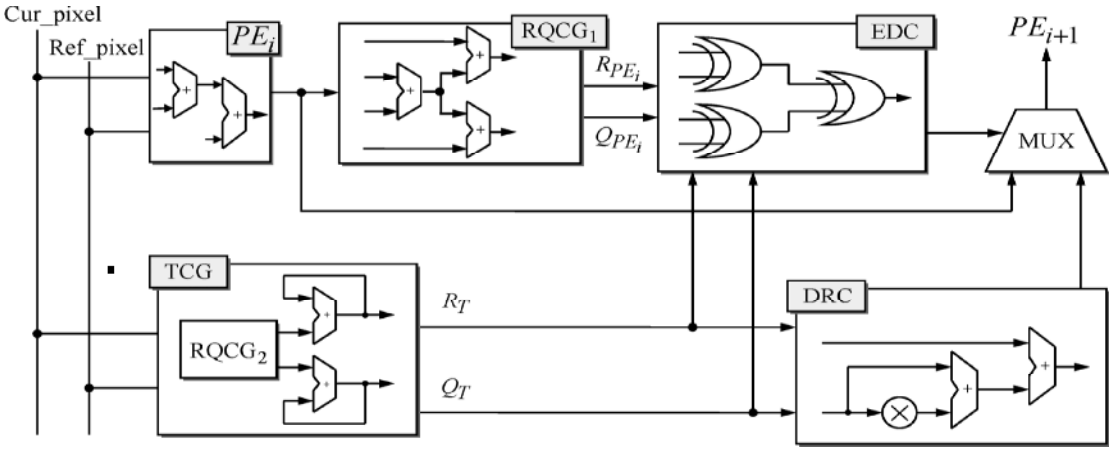

Fig.2. A specific PE_i testing processes of the proposed EDDR architecture.

estimates the absolute difference between the Cur_pixel of the search area and the Ref_pixel of the current macroblock. Thus,by utilizing PEs, SAD shown in as follows, in a macroblock with size of *NxN* can be evaluated:

$$\mathrm{SAD}=\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}|X_{ij}-Y_{ij}|$$

Where X_{ij} and Y_{ij} represent the luminance pixel value of Cur_pixel and Ref_pixel, respectively. Based on the residue code, the definitions shown in (2) and (3) can be applied to facilitate generation of the RQ code (R_T and Q_T) form TCG. Namely, the circuit design of TCG can be easily achieved (seeFig.3) by using R_T and Q_T given below.

$$R_T=\left\lfloor\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij}-Y_{ij})\right\rfloor_m$$

$$Q_T=\left\lfloor\frac{\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij}-Y_{ij})}{m}\right\rfloor_m$$

VI. ACCUMULATOR

In this module consists flip-flop act as a accumulator. We can store a bit of data. Flip-flop" is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data. There are some circuits that are not quite as straight forward as the gate circuits we have discussed in earlier lessons. However, you still need to learn about circuits that can store and remember information. They're the kind of circuits that are used in computers to store program information RAM memory.

VII. ERROR DETECTION CIRCUIT

Our proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) in utilizes the

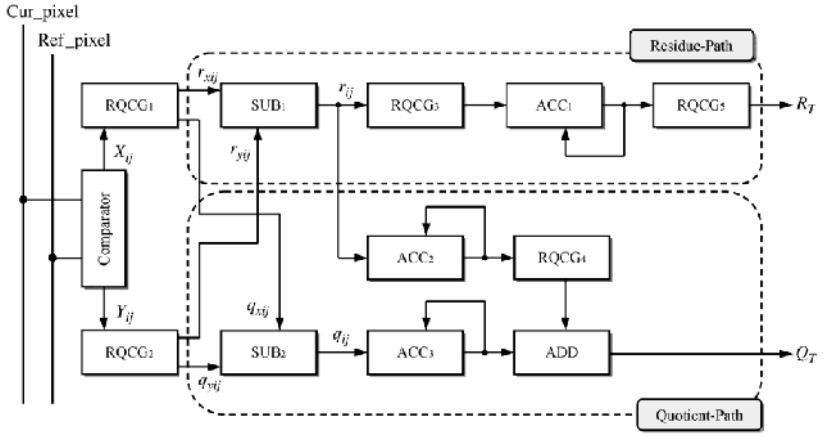

Fig.3. Circuit design of the TCG.

concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDDR scheme to detect errors and recover the corresponding data.

This work adopts the systolic ME as a CUT to demonstrate the feasibility of the proposed EDDR architecture. A ME consists of many PEs incorporated in a 1-D or 2-D array for video encoding applications. A PE generally consists of two ADDs (i.e. an 8-b ADD and a 12-b ADD) and an accumulator (ACC). Next, the 8-b ADD (a pixel has 8-b data) is used to estimate the addition of the current pixel (Cur_pixel) and reference pixel (Ref_pixel). Additionally, a 12-b ADD and an ACC are required to accumulate the results from the 8-b ADD in order to determine the sum of absolute difference (SAD) value for video encoding applications Notably, some registers and latches may exist in ME to complete the data shift and storage. For example of the proposed EDDR circuit design for a specific PEi of a ME. The fault model definition, RQCG-based TCG design, operations of error detection and data recovery.

VIII. DATA RECOVERY CIRCUIT

In this module will be generate error free output by quotient multiply with constant value (64) and add with reminder code. During data recovery, the circuit DRC plays a significant role in recovering RQ code from TCG. Notably, the proposed EDDR design executes the error detection and data recovery operations simultaneously. Additionally, error-free data from the tested PEi or data recovery that results from DRC is selected by a multiplexer (MUX) to pass to the next specific PEi+1for subsequent testing. Error concealment in video is intended to recover the loss due to channel noise, e.g., bit-errors in a noisy channel and cell-loss in an ATM network, by utilizing available picture information. The error concealment techniques can be categorized into two classes according to the roles that the encoder and the decoder play in the underlying approaches. Forward error concealment includes methods that add redundancy in the source to enhance error

resilience of the coded bit streams. For example, I-picture motion vectors were introduced in MPEG-4 to improve the error concealment. However, a syntax change is required in this scheme. In contrast to this approach, error concealment by post-processing refers to operations at the decoder to recover the damaged images based on image and video characteristics.

In this way, no syntax is needed to support the recovery of missing data. we have only discussed the case in which one frame has been damaged and we wish to recover damaged blocks using information that is already contained in the bit-stream. The temporal domain techniques that we have considered rely on information in the previous frame to perform the reconstruction. However, if the previous frame is heavily damaged, the prediction of the next frame may also be affected. For this reason, we must consider making the prediction before the errors have occurred. Obviously, if one frame has been heavily damaged, but the frame before that has not been damaged, it makes senses to investigate how the motion vectors can be extrapolated to obtain a reasonable prediction from a past reference frame. Following this notion, we have essentially divided the problem of error concealment into two parts.

The first part assumes that the previous frames are intact or are close to intact. This will always be the case for low BER and short error bursts. Furthermore, a localized solution such as the techniques presented in the previous subsection will usually perform well. However, if the BER is high and/or the burst length is long, the impact of a damaged frame can propagate, hence the problem is more global and seems to require a more advanced solution, i.e., one which considers the impact over multiple frames.

In the following, we propose an approach that considers making predictions from a past reference frame, which has not been damaged. The estimated motion information which differs from the actual one may be recovered from that of neighbor blocks. Because a moving object in an image sequence is larger than the block size of a minimal block in many occasions, motion information of neighbor blocks are usually the same as, or approximate to, current blocks. The concept of global motion is discussed in many researches on motion estimation or related interests. In method which reconstructs the frame with the aid of neighbor motion vector is successfully applied to motion estimation. Thus, an error signal “1” is generated from EDC and sent to mux in order to select the recovery results from DRC.

IX. CONCLUSION

This work presents an EDDR architecture for detecting the errors and recovering the data of PEs in a ME. Based on the RQ code,A RQCG based TCG design is developed to generate the corresponding test codes to detect errors and recover data. The proposed EDDR architecture is also implemented by using Verilog and synthesized by modelsim.

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