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DESIGN AND VERIFICATION OF ANALOG PHASE LOCKED LOOP CIRCUIT

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Abstract: This paper describes a design of phase locked loop system suitable for clock synchronization and generation. PLLs with high speed, low noise and wide bandwidth with fast acquisition time are preferred. A Phase Detector (PD) with low dead zone, charge pump with passive low pass filter and a low noise, wide tuning VCO are integrated in the PLL system. A novel voltage controlled oscillator (VCO) with wide tuning range of 141.2 MHz of frequency is designed. The PD modeled is a D-latch based digital PD and conventional charge pump with second order loop filter is used. Integrating this VCO in a PLL system offers and wide bandwidth. This PLL system is simulated and tested in CADENCE UMC180nm technology. The results prove that the lock-in range of PLL is 40MHz to 140 MHz with a maximum pull-in time is 2.19us and the maximum power consumed by this PLL system is 2.99mW at 140MHz

Keywords-Phase Locked Loop (PLL), Phase Detector (PD), Charge Pump (CP), Loop Filter, Voltage Controlled Oscillator (VCO),Frequency Divider, Lock-in range, Lock time.

INTRODUCTION

A PLL is a feedback control system which locks the reference signal to the VCO output signal when the received signal is well within the operating range of the PLL. PLL is used as on chip clock generator, frequency synthesizer and as clock and data recovery system in computer, radio and tele- communication system. A PLL with wide tuning range is desired. As the technology scale down, PLL operating at high frequencies are preferred. Conventional voltage phase detector PLLs has many drawbacks like steady state error and limited pull-in range. The design includes a charge pump PLL as it offers zero steady state phase error and infinite pull-in range. It is the VCO which decides acquisition range of PLL. For a PLL with wide acquisition range a wide tuning VCO is required. In this work, a PLL system is designed with 141.2 MHz operating range. The bandwidth of the PLL is determined by the tuning range of the VCO. But VCO is one of the main sources of jitter. A VCO with high tuning linearity, low noise and wide bandwidth is preferred. VCO offers wide tuning range but the noise at the output is also high. A novel telescopic differential amplifier based VCO with low noise and wide tuning range is designed. This VCO is preceded with a MOS device with current mirrors to make it work as VCO. Active loop filter which is another noise source can be avoided and passive loop filter with conventional charge pump can be used to generate the control voltage. This also reduces the overall system noise and power consumption.

LITERATURE REVIEW

A PLL design with operating range of 640 KHz to 800 KHz with utmost lock time 6s is proposed in work. The work presented in [2] used an opamp based charge pump to reduce the current mismatch but this consumes more power and adds noise to the overall system. Also the time taken by the PLL to lock to the reference signal is high. The VCO made up of a two stage OTA adds to the power consumption. Two stage opamp offers high gain but the circuit complexity is high. The dominant pole is decided by the external load at the output node. The output node becomes dominant only if it drives very high load. Also, the stability of two stages OTA degrades when connected in a feedback system [3]. The overall power consumption of the system is 5.14mW. The VCO designed offers a narrow bandwidth which limits the PLL operating range to few MHz [1], [2], [4] used a dynamic logic PD to reduce the power consumption. Since jitter is inversely proportional to power consumption the jitter obtained is 65ps and 30ps. [1], [2], [4] operates in MHz with narrow bandwidth and moderate power consumption. These drawbacks can be improved by using a telescopic OTA based ICO which offers wide tuning range, low phase noise and higher design flexibility [3].

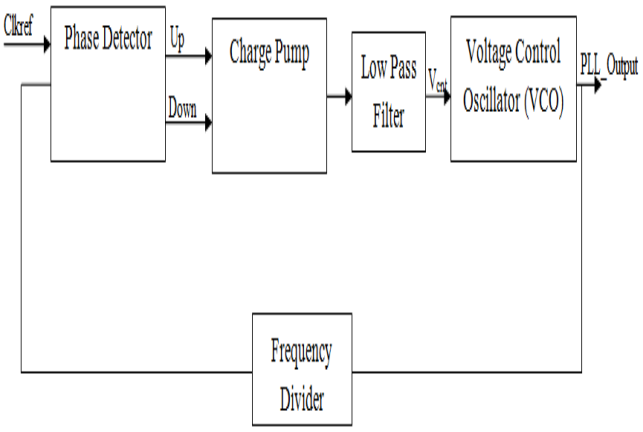

Fig 1, PLL Design

PLL DESIGN

The PLL architecture is shown in Fig. 1 and the main Components are phase detector, charge pump, loop filter, voltage controlled oscillator and Frequency Divider.

PHASE DETECTOR

PD compares the incoming signal with the PLL output and generates the phase difference as an error signal. The PD circuit should consume low power and have a minimum dead zone. Dead zone is a region wherein a PD fails to detect small phase errors. This occurs when there is very small phase difference between the reference signal and VCO output signal. The PD designed is a conventional D Latch based phase frequency detector as shown in Fig. 2. It generates UP and DOWN pulses based on the frequency

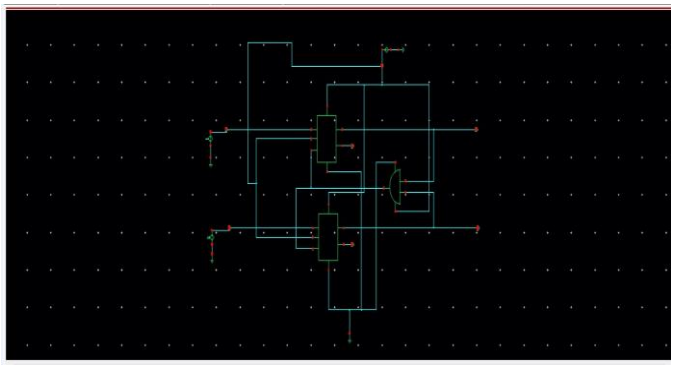

Fig 2, Phase Detector Design

CHARGE PUMP

Charge pump with loop filter provides the appropriate control voltage for the VCO to generate the required clock signal. A conventional charge pump design adapted from is shown in Fig. 3 Charge pump is driven by the UP/DOWN pulses from the PD. The UP signal charges the loop filter where as the DOWN signal discharges the loop filter, based on this the control voltage is generated. Imperfections between this PD and CP may lead to high ripple in Vcntrl. Problems in conventional charge pump design which causes Vcntrl to vary in locked state:

1. The inverter placed next to UP signal introduces delay which is compensated by placing a transmission gate after the DOWN Signal.
2. Current mismatch between the PMOS and NMOS transistors are avoided by sizing the PMOS transistor larger than NMOS.
3. Charge sharing at the drain of M5 and M2 can be avoided by connecting a bootstrap buffer.

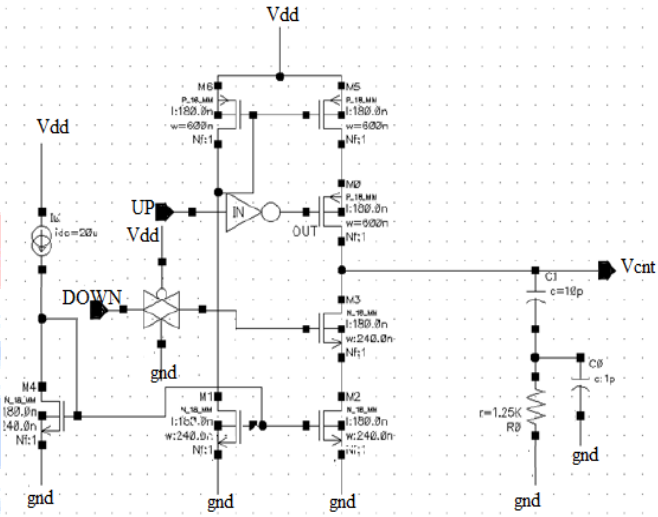

Fig 3,Charge Pump Design

The output control voltage of the charge pump is given by Eqn. 1, V_C (t) is the control voltage, Icp is the output current, Ccp1 is the output capacitance and ΔΦ is the phase difference between the two signals.

$$Vc(t) = \frac{\text{Icp}}{2\pi\text{Ccp1}}\text{t}.\Delta\emptyset \qquad \text{Eqn.1}$$

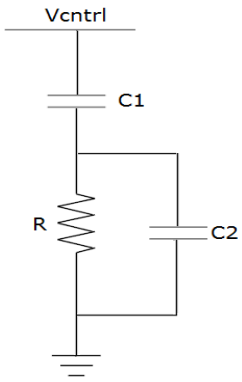

Fig 4, Low Pass Filter

LOOP FILTER

Loop filter eliminates the undesirable high frequency components and retain the dc level of the generated control voltage (Vcntrl). It also determines the stability of the system. Active loop filters offer wide output swing at the cost of increased device noise and high power consumption. A passive second order RC filter shown in Fig. 4 is used. The resistance in series to output capacitance C1 adds a zero to the transfer function to improve the stability of the system. A capacitance C2 is added in parallel to the resistance to control the ringing of the output voltage at high frequencies.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

A simple oscillator produces a periodic output, usually in the form of voltage. As such the circuit has no input while sustaining the output indefinitely.
A Voltage Controlled Oscillator or VCO is a circuit whose output frequency is linear function of its control voltage

The applied control voltage determines the instantaneous oscillation frequency. Consequently, modulating signals applied to control input may cause frequency modulation (FM) or phase modulation (PM). A VCO is a part of a phase-locked loop.

DIFFERENTIAL AMPLIFIER

Building a two-stage differential amplifier can achieve a much higher gain through the cascade of two amplifiers, a single ended differential amplifier and a common source amplifier. The other performance criteria remained the same as the single stage differential criteria. However stability criteria were specified to account for the need to stabilize the system that now has two poles.

The requirement here is that of a high gain amplifier which is used to maintain the voltage across the NNMOS by tuning the current in the tail current source. We design a 2 – stage op-amp (differential amplifier) with the first stage being a differential amplifier with NMOS input pair and PMOS diode connected load. The second stage consists of a common source amplifier with a high output resistance to achieve high gain. The overall gain of this opamp is given by

$Av = gm*R_0$

Where,

R_0 → output impedance.

gm → transconductance of the input NMOS.

The architecture of the amplifier uses a basic differential amplifier with NMOS input for bias voltage (control voltage) and a two ended output along with a two inputs. It contains 2 PMOS and 2 NMOS. The schematic of the design is shown in Fig 5.

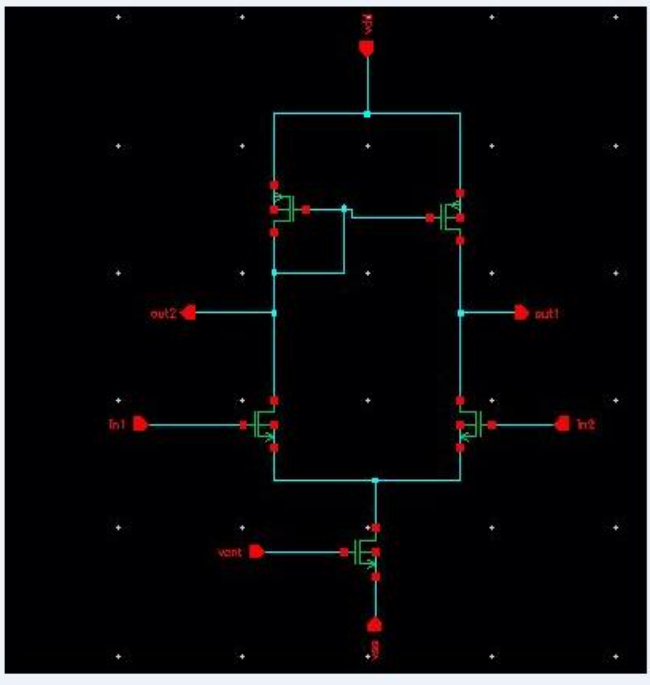

Fig 5,Differntial Amplifier

The above fig 5 shows the differential amplifier circuit then designing a symbol and four blocks are design from the amplifier connecting all the blocks in the form of a ring to ensure that we get a phase difference of 180 degrees, and to achieve desired frequency. The major tuning parameters are the gm (or W/L) of load for the required frequency and the gm (or W/L) of the input NMOS to get the required gain greater than unity.VCO circuit is shown in Fig 6. According to design specification of 141.2MHz oscillation frequency has been achieved.

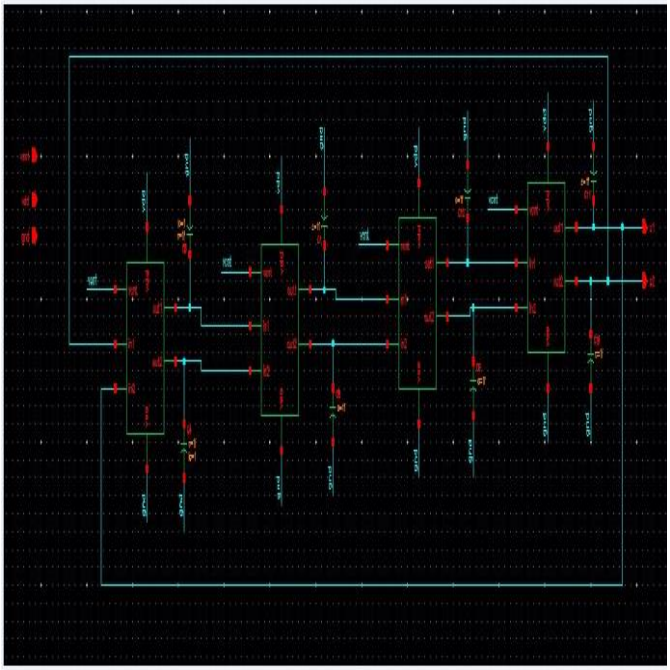

Fig 6, VCO Design

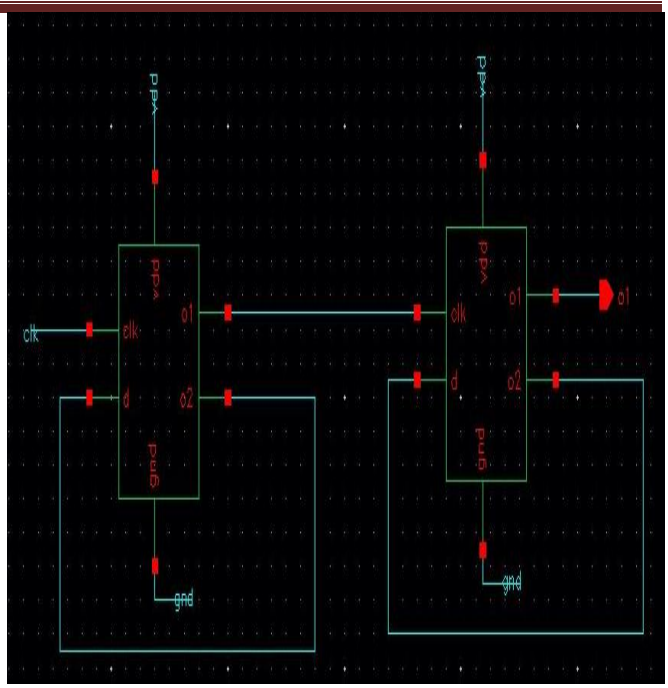

Fig 7,Frequency Divider

FREQUENCY DIVIDER

Frequency divider circuit is a VLSI phase scaling circuit. It is responsible to down-convert the frequency of an input signal to a lower value. We can achieve programmability in the output frequency by using a programmable frequency divider circuit. Phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. In our case a 1\4 frequency dividers that operate for a supply voltage of 1.8V are used.

We have used the Positive edge D flip flops for the design of the flip flop present in the frequency divider. Positive edge D flip flop is insensitive to clock overlaps or skew. Therefore, the possibility of sampling error due to timing variation of clock edge of flip-flop in high speed operation is eliminated.

The architecture becomes simple compared to flip-flop or SR latch using one with lower power consumption and area. In our Design, the frequency division factor depends upon Rate select signal. Based on the output frequency we have designed 1/4 dividers. We have used the D flip flop based designed for all the frequency dividers. Divide by 4 are implemented using 2 individual frequency dividers namely ½ schematics as shown below Fig 7.

SIMULATION RESULTS AND DISCUSSION

The proposed PLL system is simulated in CADENCE UMC180nm Technology. The output clock generated for a frequency of 141.2 MHz is shown in Fig.8. The time taken for the PLL to lock to the reference frequency is 2.199us. The control voltage for this frequency is 1.7 V and is stable in the acquisition period.

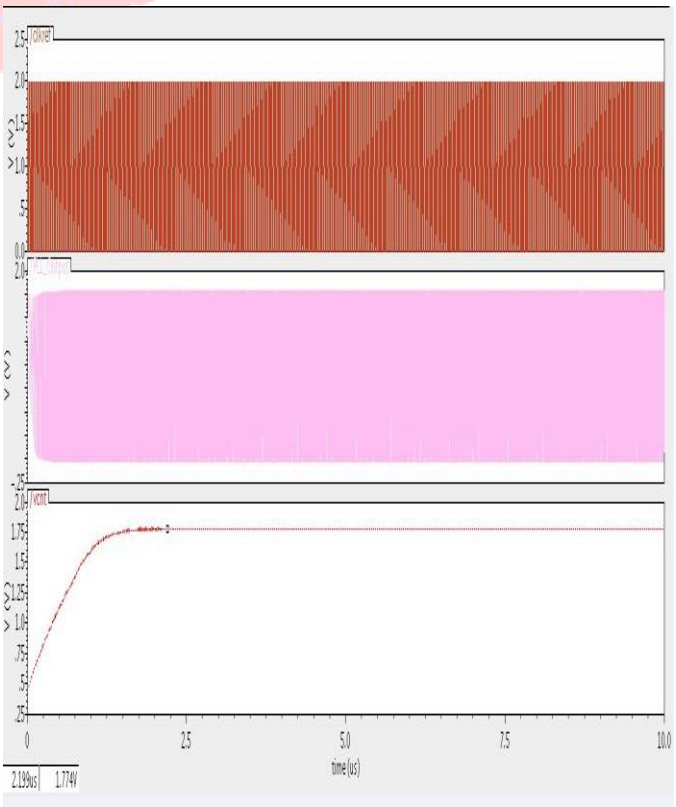

Fig 8,PLL Result

The PLL output and the reference signal under locked state are shown in Fig.9. The PLL pull in time is 2.199us and capture range is 40 MHz to 140 MHz

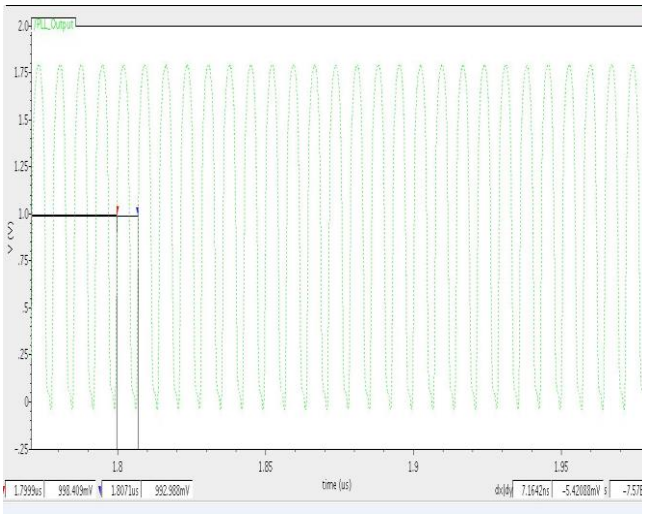

Fig 9,PLL Output

CONCLUSION

The focus of this project is to design a 141.2MHz range of PLL with low power consumption. A telescopic differential amplifier based on VCO is designed to improve the lock-in range and make the PLL operate at high frequency. A conventional charge pump is designed and the problems of current mismatch between the charging and discharging current are minimized. This improves the performance and a D-latch based PD and passive loop filters are used to reduce the overall power consumption and improve the system stability. The major power consuming block in the proposed system is VCO. The system is simulated in CADENCE UMC180nm technology and the results obtained shows that the lock-in range is 141.2 MHz and maximum lock range 0f 2.19us with 2.99mW power consumption.

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